



*BSDArchitect is a powerful boundary scan insertion tool that can generate nearly any boundary scan configuration.*

### SAVES WEEKS IN ASIC AND IC DESIGN

The BSDArchitect™ boundary scan tool is designed to dramatically reduce development time for ASIC and IC designs by automating the otherwise tedious process of implementing boundary scan circuitry.

BSDArchitect provides a flexible test access port (TAP) that supports almost any boundary scan configuration, from the simplest implementation for board manufacturing test to a full system-on-chip (SoC) level test controller, including all pre-defined and any number of private instructions. This is particularly important for SoC designs, where simple access is needed to test internal structures, such as memory and logic built-in self-test (BIST), embedded cores and internal status registers.

### TECHNOLOGY-SPECIFIC BOUNDARY SCAN CELLS AND I/O PADS

Many technologies provide boundary scan cells optimized to meet a design's performance requirements. BSDArchitect automatically inserts these technology-specific cells into the design.

Advances in IC design and packaging technology mean that ICs can have thousands of pins configured in complex packages. BSDArchitect automatically generates technology-specific I/O pads connecting to every port on the design. It also supports complex I/O pads, such as open collector and low voltage differential cells.

The technology mapping features of BSDArchitect facilitate RPCT for testing designs with a large number of I/Os or using less expensive, low pin count testers.

### AUTOMATION

- Generates IEEE 1149.1-2001 compliant boundary scan circuitry and boundary scan design language (BSDL) for complete automation of boundary scan design

### FLEXIBILITY

- Enables user-specified boundary scan configurations for maximum flexibility
- Inserts technology-specific boundary scan cells and I/O pads to meet design-specific requirements
- Supports Reduced Pin Count Testing (RPCT) for low cost test

### DESIGN FLOW

- Interfaces to memory BIST, internal scan, logic BIST and other SoC test structures, providing whole chip test control
- Supports designs at the register transfer level (RTL) or gate level for ease of design flow
- Creates verification test benches, including BSDL compliance checking, for quick and easy verification
- Generates cyclized patterns for application on tester, such as STIL and WGL



## SOC TEST CONTROL

BSDArchitect provides a comprehensive solution for testing embedded structures such as memory BIST, internal scan, and logic BIST without the need to bring test control signals to top-level chip I/Os. The tool builds on its support for private instructions to generate test data registers and design objects that interface the embedded test structures to the TAP.

BSDArchitect creates the logic and registers required to control the internal test structures and provide access to the results through the TAP interface. The same structures can be used to set up and observe other SoC test modes, such as port constraints for automatic test pattern generation (ATPG) sessions and control of multiple BIST controllers. BSDArchitect uses only IEEE 1149.1-2001 compliant structures for the BIST interface and supports the Mentor Graphics MBISTArchitect™ tools, third-party, and manually created test structures.

## COMPREHENSIVE VERIFICATION TEST BENCHES AND TEST VECTORS

BSDArchitect supports a complete flow for verifying the functionality and compliance of the generated circuitry. The tool reads IEEE standard BSDL files and creates test benches and test vectors for verifying boundary scan logic, even for third-party boundary scan designs.

One of the key features of BSDArchitect is the ability to verify the functionality of internal test structures, such as BIST, through the TAP interface. BSDArchitect creates test benches and cyclized test vectors, such as STIL and WGL, for running and verifying the test. This ensures that the TAP interface works correctly for all configurations.

BSDArchitect automatically creates DC parametric tests as part of the boundary scan generation process. Because the tool understands the boundary scan configuration, it generates these tests in a matter of seconds.

## DESIGN FLOW AND DFT INTEGRATION

BSDArchitect fits into any standard Verilog or VHDL design flow. The tool can read a design at either the RTL or gate-level and can handle designs with or without existing I/O pads.

Based on the user's specification of the boundary scan configuration, BSDArchitect generates the boundary scan circuitry as synthesizable RTL, compliant with any standard logic synthesis product.

BSDArchitect generates a correct-by-construction BSDL file that can be used by test generation tools for board or system test. The tool also generates a number of drivers for the downstream verification process, such as simulation vectors for use with the FlexTest™ fault simulator, and drivers for running ATPG on the design using the Mentor Graphics TestKompress® or FastScan™ tools. BSDArchitect includes all the necessary interfaces to smoothly integrate to Mentor's MBISTArchitect for memory BIST and LBISTArchitect™ for logic BIST.

BSDArchitect is part of the Mentor Graphics technology-leading DFT tool suite, which includes integrated solutions for scan, ATPG, Test time/data compression, advanced memory test, logic BIST, boundary scan, diagnosis, and a variety of DFT-related flows. All Mentor DFT tools are available on UNIX and Linux platforms. For more information, visit [www.mentor.com/dft](http://www.mentor.com/dft).

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