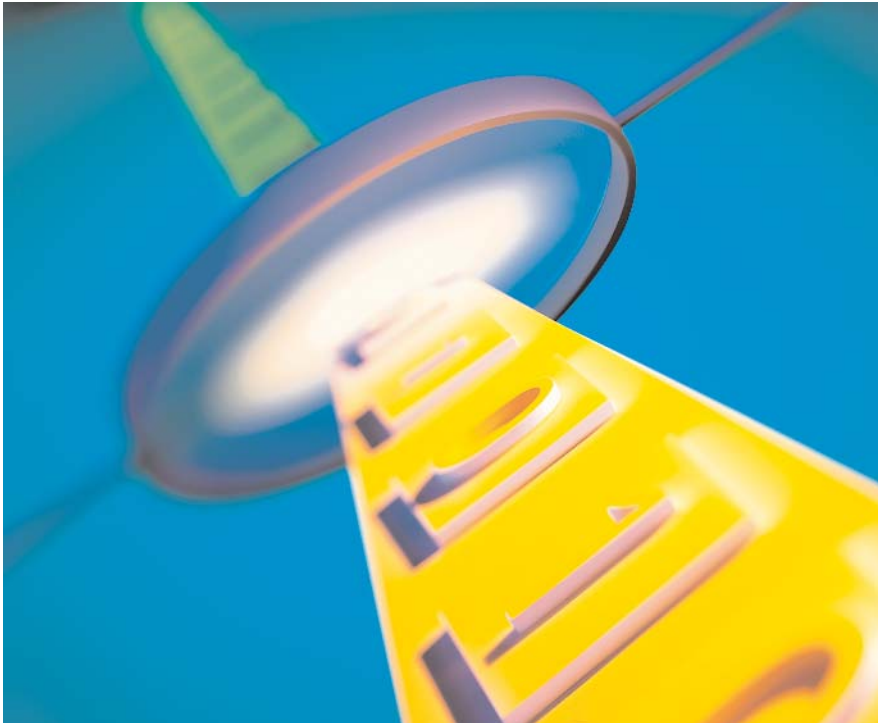


LBISTARCHITECT

LOGIC BUILT-IN SELF-TEST

Design-for-Test

D A T A S H E E T



LBISTArchitect provides a complete environment for logic BIST design.

ELIMINATING STORED PATTERNS

LBISTArchitect™ is the Mentor Graphics Design-for-Test (DFT) logic built-in self-test (BIST) product. For applications requiring a vector-less test approach, such as in-system test, LBISTArchitect offers a complete solution for analyzing test structures into the design's fault coverage and reference signatures.

Rather than using a tester to apply external patterns, LBISTArchitect uses a BIST methodology to embed much of the test functionality into the device itself. A BIST controller is inserted into the design that essentially applies a series of scan patterns, as an external tester would, except the patterns are generated and the responses are captured on-chip. This allows the tests to run in environments where a tester is not connected to the device.

IMPROVED TEST QUALITY WITH AT-SPEED PATTERNS

High test quality—the ability of the test to screen out defective parts—is the most important factor affecting the choice of DFT methodology and tools. High fault coverage is critical to ensuring that defective devices are identified and isolated during the test process.

LBISTArchitect's patented test point insertion technology ensures high fault coverage for BISTed designs. In addition, the BIST controller is specifically designed to target faults traditional BIST implementations might overlook.

As designs migrate to sub-100 nanometer feature sizes, “at-speed” test has become a critical requirement to ensure high test quality. LBISTArchitect supports at-speed testing by generating a BIST controller that handles

HIGH TEST QUALITY

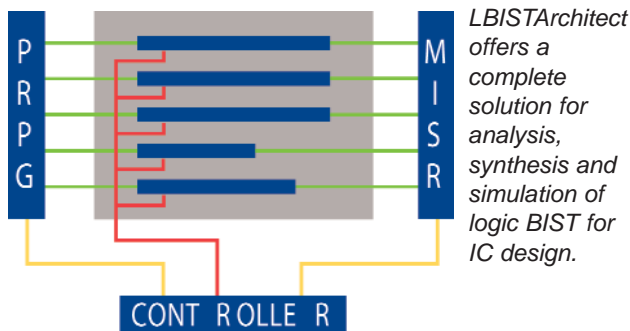
- Very high fault coverage maximizes product quality and minimizes field returns
- At-speed BIST for improved test quality
- Patented MTPI™ test point insertion algorithms maximize fault coverage with minimal impact on the design itself

COMPREHENSIVE FLOW

- Comprehensive BIST-Ready capabilities, including BIST DRCs and automatic resolution of BIST violations
- ECO immunity saves weeks in design implementation time by removing the need to re-implement BIST during place-and-route iterations
- Fast fault simulation and signature generation, including intermediate signatures, aid diagnosis and debug
- Supports Hierarchical BIST in conjunction with BSDArchitect™
- Completely compatible with FastScan™ ATPG—identical libraries fault classifications, and simulation engines



multiple clock frequencies at arbitrary relationships. The fully customizable controller can lead the scan chains at a slower frequency to reduce power dissipation while testing all paths at-speed during user-configurable capture windows. Additionally, in order to minimize the timing and routing requirements on scan enable, LBISTArchitect turns off all clocks at the end of the shift cycle allowing scan enable to settle before starting the capture cycle.



LOW IMPACT TEST LOGIC WITH TIMING CLOSURE

LBISTArchitect uses a simple Multi-Phase Test Point Insertion (MTPI) technology to maximize a design's fault coverage while minimizing the impact on the design's area, routing, and critical timing. MTPI adds control and observe points to ensure that areas of the design that are difficult to test using BIST patterns become testable. The MTPI methodology, however, uses only one-tenth the area overhead of traditional methods and ensures that test points are not added to timing critical areas or paths within the design.

BIST-READY CAPABILITIES AND FLOW

One of the most time-consuming aspects of BIST implementation lies in ensuring that the core design itself is testable and that target fault coverage goals are met. LBISTArchitect's "BIST-Ready" process analyzes the design for testability issues and automatically corrects BIST-related problems. The tool contains more than 150 design rule checks (DRCs), analyzing the design for

clocking issues and scanability problems. LBISTArchitect also identifies and automatically corrects for X generators, structures that can cause the BIST controller to become corrupted during test mode. The DRC violations can be displayed graphically to help identify the cause and associated remedy of the problem.

LBISTArchitect also bounds the design's primary inputs and outputs in a way that maximizes fault coverage and ensures that the BISTed design or core can be reused in any application. It also allows design blocks and cores to be independently BISTed and integrated into an SoC design without affecting test operation.

LBISTArchitect synthesizes the logic BIST controller, together with its connection to the core design, as a register-transfer level (RTL) object in either VHDL or Verilog. The tool generates multiple drivers to aid downstream processes of logic synthesis, fault simulation, boundary scan implementation, and signature verification.

LBISTArchitect provides fault simulation, fault analysis, and signature calculation for the BISTed design. LBISTArchitect also provides mechanisms to debug a design's fault coverage. In order to improve fault coverage, the fault analysis, including graphical display of results, analyzes undetected faults and identifies why they were not detected. As part of the fault simulation, in addition to calculating the BIST controller's fault free signature, LBISTArchitect also calculates intermediate signatures. These intermediate signatures are useful during fault diagnosis, debug and failure analysis.

LBISTArchitect is part of the Mentor Graphics technology-leading DFT tool suite, which includes integrated solutions for scan, ATPG, Test time/data compression, advanced memory test, logic BIST, boundary scan, diagnosis, and a variety of DFT-related flows. All Mentor DFT tools are available on UNIX and Linux platforms. For more information, visit www.mentor.com/dft.

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03/2006 1024530-w
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