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Launch-off-shift at-speed test

A comparison of broadside-transition-pattern and launch-off-shift techniques shows the latter to be viable for testing a 90-nm wireless baseband device.

By Noam Benayahu and Arik Chechik, Metalink, and Ron Press, Mentor Graphics -- *Test & Measurement World*, 6/1/2007

Both launch-off-shift (LOS) and broadside-transition-pattern techniques are finding use in the at-speed test of devices fabricated in 130-nm processes and below. The broadside-transition-pattern approach is most commonly used, but our experiments in applying both techniques to the test of a wireless baseband device show that LOS can provide advantages.

[Learn more about scan technology.](#)

At-speed scan test serves applications for which static testing is not sufficient ([Ref. 1](#)). The basic operation of at-speed scan testing involves loading the scan chains at a slow clock rate and then applying two clock pulses at the functional frequency ([Figure 1](#)). The first pulse causes a transition to start propagating from a scan-cell. The second pulse captures the scan cell value at the end of the path being tested.

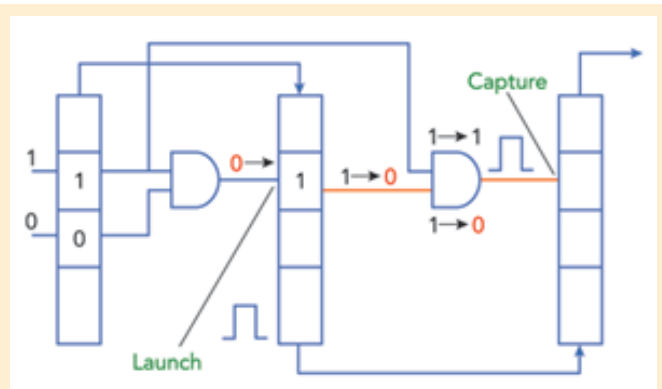


Figure 1. At-speed scan test involves loading scan chains at a slow clock rate and then applying two clock pulses at the functional frequency.

If the circuit is operational, then the transition will propagate to the end of the path in time and the correct value will be captured. Otherwise, if a delay causes a slow propagation, the transition from launch to capture cell will be slow, an erroneous value will be captured, and the defect will be detected.

The most popular at-speed scan pattern is the transition pattern (Ref. 2). A potential fault of slow to rise (0 to 1) and slow to fall (1 to 0) is modeled at every gate terminal within the design. Automatic test-program generation (ATPG) tools target these fault sites and cause a transition using any launch scan cell and capture results using any downstream scan cell.

Using PLLs for accurate clocks

A fundamental problem with at-speed scan testing is how to apply accurate clocking for the at-speed launch and capture pulses. Traditional stuck-at scan patterns are static. Stuck-at clocking for loading the scan chain and capturing results is often performed at frequencies between 10 MHz and 40 MHz. At-speed scan testing can load the scan chains with a clock frequency that is similar to the one used for stuck-at tests, but the launch and capture pulses must be applied at the functional frequency.

Supplying the at-speed clock for launch and capture from a tester becomes more demanding as the desired frequency increases. A solution of using some basic programmability around device internal phase-locked loops (PLLs) provides a nice option (Ref. 3). Providing internal PLL control for at-speed test has become a common practice for at-speed scan testing (Refs. 4 and 5).

The most common technique for applying at-speed transition patterns is referred to as a broadside or launch-from-capture pattern type (Ref. 6), as shown in Figure 2. With this pattern type, the scan chain is loaded and then placed in functional/capture mode by forcing scan_enable (SE) to 0. Sometimes, an extra cycle is added to the test pattern that has no activity to ensure that the scan_enable completely settles. Next, two pulses are generated to launch and capture the transition.

The broadside pattern launches the transition in the functional mode of operation, so it is likely to propagate transitions along paths that are real functional paths. Often, the coverage report from broadside pattern ATPG can be 10% lower than standard static stuck-at patterns.

Launch-off-shift patterns

With LOS patterns (Figure 3), the launch occurs during the last shift while loading the scan chain. Next, the circuit is placed into functional/capture mode very quickly so an at-speed functional clock can be pulsed.

ATPG is much easier with LOS compared to broadside patterns. It is a simple ATPG activity to load the starting value for a transition directly to the scan cell one shift before the last and then load the transition value in the last shift. Broadside patterns require ATPG to calculate the transition value through the combinational logic, since it is in functional mode during the launch pulse. In addition, LOS patterns usually report higher coverage than broadside patterns.

LOS reports higher coverage and is easier for ATPG, so it results in fewer patterns and faster ATPG run times compared to broadside patterns. So, why is broadside transition test more popular than LOS patterns?

There are two primary reasons for the reluctance to use LOS patterns. The first is the difficulty to make the circuit change from shift mode to functional/capture mode between the last shift and functional clock pulse. If standard scan_enable architecture is used, then the scan_enable must be routed as a clock. Furthermore, since scan_enable goes to all sequential elements, it is a global clock and must settle at the system clock frequency. One way to work

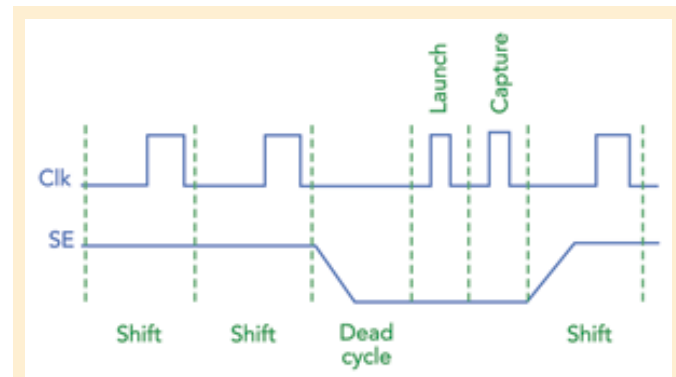


Figure 2. With broadside transition patterns, a scan chain is loaded and then placed in functional/capture mode by forcing scan_enable (SE) to 0.

around this issue is to add pipelining logic throughout the device for scan_enable (Ref. 7).

Pipelining scan_enable adds additional test logic to the design, but it removes the difficult task of treating scan_enable as a global clock. As shown in Figure 4, the clock triggers a change within the local scan_enable.

The other common concern with LOS patterns is that they may test the circuit through paths that are not possible functionally. LOS patterns can shift in a transition that is impossible during normal circuit operation.

An important question to ask is how much of the additional coverage beyond broadside patterns is due to nonfunctional logic? It's possible that testing nonfunctional logic during at-speed tests will falsely report failures and result in yield loss (Ref. 8).

Accounting for false and multicycle paths

During the design process, many paths are determined to be either false or multicycle paths. A standard Synopsys Design Constraints (SDC) file lists false and multicycle paths such that special efforts are not made for timing closure at these paths. Two types of false paths can exist. Some false paths cannot be sensitized and are not possible during functional operation (but may be possible during scan mode). The other types of false paths are paths that are not intended to operate at system frequencies. Multicycle paths require more than one functional clock cycle to propagate.

Both false and multicycle paths must be considered during at-speed scan testing. Scan has the potential to directly load scan cells into a circuit state that isn't possible during functional operation. As a result, false or multicycle paths may be activated during at-speed scan testing. If the at-speed scan tests fail due to these paths, then correctly functioning devices may be falsely discarded. The result could be yield loss.

To avoid such loss, engineers have often tested for false and multicycle paths during time-based simulation and test program tester integration, and they have often performed these tasks manually.

Fortunately, automation has been added to ATPG tools so they can now directly read standard SDC files and extract the timing-exception path information (Ref. 9). With this automation, if a test propagates a signal along a false or multicycle path that is sensitized during ATPG, then the capture scan cell will capture an unknown X value.

Baseband-chip case study

Metalink, a company that designs wireless and wireline broadband communication chips, needed to develop an effective test strategy for its WLANPlus 802.11n-draft-compliant wireless LAN technology, which is optimized for the networked home entertainment environment. The company's WLANPlus family consists of the MtW8171 baseband device and the MtW8151 RFIC. The MtW8171 baseband chip is manufactured at a 90-nm low-power process and implements full at-speed scan-test capability. For this device, at-speed scan was implemented using both LOS and broadside transition patterns.

To reduce the increased pattern count required to cover transition faults, we implemented compression logic using Mentor Graphics

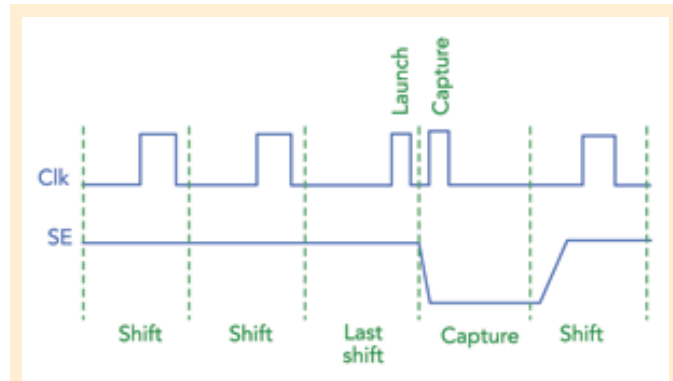


Figure 3. In a launch-off-shift transition pattern, the launch occurs during the last shift while loading the scan chain.

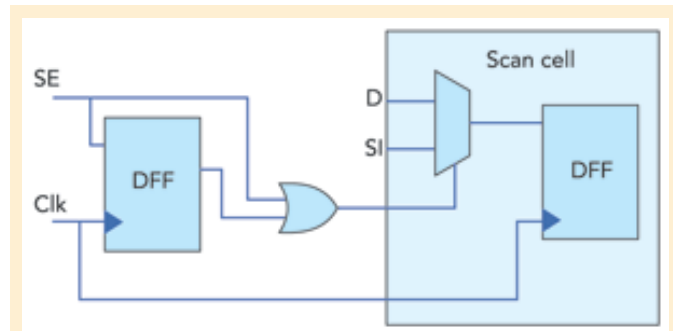


Figure 4. Pipelining scan_enable adds additional test logic to the design, but it removes the difficult task of treating scan_enable like a global clock.

Embedded Deterministic Test technology. The bring-up of the scan program for this chip took only two days from the chip arrival to the moment where all bring-up patterns were up and running at-speed.

We performed experiments to compare the difference between broadside and LOS coverage. We generated the initial patterns by using procedures that define specific clock sequences that can be used.

Table 1 shows the results of transition pattern generation. Initially, the LOS patterns reported 78.57% test coverage compared to 71.38% for broadside patterns. Thus, LOS appeared to test >7% more faults. Next, we considered false and multicycle paths, since these paths are not intended to operate at functional clock rates.

After accounting for false and multicycle paths (MCPs), the LOS and broadside coverages were reduced to 72.88% and 69.55%, respectively. Therefore, 5.69% of faults reported in the initial LOS detection were false paths and MCPs. Similarly, 1.83% of broadside detection was due to false paths and MCPs. Based on these results, we concluded that a significant portion of the advantage in test coverage with LOS patterns are due to false-path and MCP testing.

These results imply that when effective false and multicycle paths are considered for LOS patterns, the risk of overtesting is reduced. As a result, LOS can be an attractive ATPG approach for at-speed test. Pattern-generation time and pattern count can be significantly smaller than broadside patterns with similar coverage. The combination of pipelined scan_enable and false and multicycle path consideration solve the most common concerns with LOS patterns. Broadside patterns should still be used to top-off coverage since LOS patterns will be unable to detect some faults.

What's next?

Manufacturers are continuing to look for ways to improve the effectiveness of at-speed scan testing. One approach, referred to as “timing-aware” ATPG ([Ref. 10](#)), targets small delay defects. It attempts to test each fault by propagating the transition down as slow a path (smallest slack) as possible. In this technique, the at-speed test pattern set is more likely to detect small defects that could escape a normal transition test set.

Another new approach to at-speed scan testing is to apply a series of at-speed shifts just before the launch cycle. Such “BurstMode” ATPG ([Ref. 11](#)) helps the at-speed clock pulses behave more like functional frequency pulses. It lessens the drooping of the voltage supply caused by the sudden pulsing of at-speed clocks for launch and capture during normal transition tests. False and multicycle path handling should be considered with both of these techniques to avoid the risk overtesting.

Meanwhile, techniques such as pipelined scan_enable make LOS more feasible, allowing users to evaluate the trade-offs between the two transition pattern types and determine which is the best solution for them. Broadside patterns offer less logic insertion and less nonfunctional path tests, while LOS patterns offer faster pattern generation and fewer patterns. The LOS approach may also be desirable for companies that are interested in detecting any type of defect, including those that are nonfunctional. Fortunately, the common concern with overtesting can be alleviated by ATPG tool handling of false and multicycle paths through SDC files that are common in design flows.

Table 1. Comparison of broadside and launch-off-shift

	Broadside	Launch-off-shift
Initial coverage	71.38%	78.57%
With SDC	69.55%	72.88%

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REFERENCES

1. Benayahu, N., et. al., "**Scan basics**," sidebar accompanying this article.
2. Saxena, J., et. al., "Scan-Based Transition Fault Testing: Implementation and Low Cost Test Challenges" *Proceedings of the International Test Conference 2002*, IEEE Computer Society Press.
3. Bailey B., et. al., "Test Methodology for Motorola's High Performance e500 Core Based on Power-PC Instruction Set Architecture," *Proceedings of the International Test Conference 2002*, IEEE Computer Society Press.
4. Boyer, J., and R. Press, "Easily Implement PLL Clock Switching for At-Speed Test," *Chip Design Magazine*, February/March 2006. www.chipdesignmag.com/display.php?articleId=376&issueId=15.
5. Beck, M., et al., "Logic Design for On-Chip Test Clock Generation—Implementation Details and Impact on Delay Test Quality," Design Automation and Test in Europe 2005. date.eda-online.co.uk/proceedings/papers/2005/year.htm.
6. Haioun, E., et al., "At-Speed Scan Transition and Path Delay Testing Using On-Chip PLL for High Frequency Device and Low Frequency Tester," Euro DesignCon 2005, www.iec.org/events/2005/euro_designcon.
7. "Use of Registered/Pipelined Scan Enable for At-Speed Testing in FastScan/TestKompress," Mentor Graphics, April 2006.
8. Rearick, J., "Too Much Delay Fault Coverage Is a Bad Thing." *Proceedings of the International Test Conference 2001*, IEEE Computer Society Press.
9. Vorisek, V., et al., "Improved Handling of False and Multicycle Paths in ATPG," *Proceedings of the 24th IEEE VLSI Test Symposium (VTS 06)*, IEEE Computer Society Press.
10. Linn, X., et al., "Timing-Aware ATPG: A Novel Test Generation Method for High-Quality At-speed Test," ATS 2006, the Fifteenth Asian Test Symposium, ats06.cs.ehime-u.ac.jp.
11. "ITC: LogicVision debuts ScanBurst, teams with Mentor," *Test & Measurement World*, October 26, 2006. www.tmworld.com.

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