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DESIGN-FOR-TEST TECHNIQUES FOR TOTAL TEST QUALITY

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With Design-For-Test (DFT), test coverage is the typical yardstick used to gauge the quality of the manufacturing tests being performed. But as next-generation designs become more complex, traditional test techniques are not sufficient.

The purpose of manufacturing test is to find defective product prior to shipping it to end-customers. The bottom line is how many of the defective parts can be detected during manufacturing test; or conversely, how many defective parts go undetected — test escapes. Traditional test approaches include static stuck-at automatic test pattern generation (ATPG) for random logic and memory built-in self-test (BIST) for large memory devices. Functional patterns are also commonly used to test the overall IC for speed-related defects.

Stuck-at patterns only detect static faults, and traditional memory BIST may not detect all potential memory faults. However, the population of at-speed types of defects is increasing in ICs. Functional at-speed pattern sets have been the standard solution to detect at-speed defects, but the practicality of developing, applying and analyzing the coverage of functional patterns is an increasing and expensive problem.

Memory BIST is and will likely remain the standard test approach for large memory. One issue with memory BIST is what to do when the memory being tested is small. It is difficult to justify the area, routing and performance impact of memory BIST for small embedded memory that are commonly dispersed throughout designs today.

These small memory require specific pattern types to test for common memory defects. They might be used for register files, FIFOs and small performance-critical memory where it is unacceptable to alter functional paths in any way.

The historical approach to testing small memory was to ignore them and accept a loss in quality, or manually create functional patterns. The resulting poor test quality could result in inverse career opportunities. Manual pattern creation would often require months of effort and could account for the crazy look that some people got.

A test technique called vector translation was developed to provide an automated method of applying specific patterns to small, embedded memory. Vector translation allows the user to define a pattern sequence and convert the pattern desired at the small memory (macro) into a scan pattern. As a result, special tests, such as a shortened March algorithm, can easily be applied without adding any logic.

Vector translation can be utilized to apply specific tests to any embedded block. Processes within vector translation can even handle testing synchronous memory using the same clock.

While random logic must be tested for static and at-speed faults, embedded memory needs to be tested for static and at-speed faults. Traditionally, the fastest application of memory BIST is to run it from the system clock, referred to as at-speed memory BIST. However, the BIST control logic normally uses the system clock to control operations and requires several cycles to perform a read or write. Consequently, at-speed memory BIST may not perform read-and-write cycles as the chip would in normal operation. A

technique to perform a more effective test is possible by pipelining the write or read operations. This is called full-speed memory BIST. Full-speed BIST can perform a write or read operation in one system clock cycle. This will detect problems with slow transitions that traditional approaches cannot.

The purpose of test is to detect potential defects, so it's desirable to have the best test coverage possible. The best way to really predict the defect levels— defective parts shipped vs. all parts shipped — is to know the probability of various defect types and the test coverage of each. This is best but usually not practical. Companies need to work out acceptable defect-level guidelines and then estimate test coverage requirements accordingly.

High-quality test is a critical part of IC manufacturing and is necessary to avoid shipping many defective parts. Acceptable test approaches of the past are no longer effective in many cases due to the increase in time-based defects. Therefore, more sophisticated and automated at-speed techniques are being utilized in IC testing for both random logic and memory. These advanced test techniques include at-speed ATPG, full-speed memory BIST and synchronous vector translation. ■

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