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Traveling at the speed of memory

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The semiconductor industry's move to nanometer technologies has brought about a rethinking of the manufacturing test process. With initial yields that can be significantly lower than those achieved at larger process technologies and the emergence of new fault types, manufacturing test will play a more important role in ensuring product quality. Traditionally, test technology has focused on the logic portion of the design. However, the International Technology Roadmap for Semiconductors 2000 has shown that it is common for today's designs to consist of more than 50 percent embedded memory, and this proportion is expected to increase in coming years. Clearly, a high-quality memory-test strategy is necessary for achieving a comprehensive system-on-chip (SoC) test.

The compact features of memory structures make them more susceptible to different types of defects. Memory array operation is primarily analog in nature. Weak signals from storage devices are amplified to appropriate drive strengths. A memory cell's signal transfer deals with small amounts of charge. These design characteristics make memory arrays more susceptible to subtle manufacturing flaws. The tight packing of memory arrays creates situations in which the state of neighboring cells can influence faulty operation in the presence of defects. Therefore, some defects can only be exposed by particular data patterns. Further, many of these defect types have a time-dependent nature, and therefore may only be seen when normal operating frequencies are applied.

Memory built-in self-test (BIST) is the standard technique for testing the embedded memories in SoC designs. It provides thorough testing of individual embedded memories with reasonable area overhead. The most common type of memory BIST consists of a finite state machine (FSM) performing three basic operations: writing patterns to the memory, reading them back and comparing them to the expected results. To access the embedded memory, the memory BIST typically inserts test muxes into the address, data and control lines. The most common types of tests performed by memory BIST are "March"-type algorithms, which will detect most of

the common memory faults, including stuck-at, addressing failures and coupling problems.

A set of March algorithms has been developed and, in most cases, forms the core of an efficient set of embedded-memory tests. However, as SoC designs move to nanometer technologies, manufacturers are concerned about the ever-increasing number of memory defects that escape these standard tests. For this reason, memory test engineers are continually developing new variations of the March algorithms. This trend will surely continue as memory sizes shrink and new memory architectures are developed. It is imperative that memory BIST tools allow sufficient flexibility to keep pace with this trend.

New at-speed test challenges

Many companies are finding that at-speed testing of all embedded memories is required to maintain an acceptable DPM (defects per million) level. It is only with at-speed testing that they can be confident that the memories will function properly during normal operation in the end application. Many implementations of the memory BIST structure may not run at-speed with embedded memories that run at higher frequencies. Fortunately, some recent advances in memory BIST technology allow at-speed algorithm use, even for memories approaching 1-GHz operating speeds.

A significant improvement that achieves at-speed memory BIST operation is the use of pipelining. It offers several key advantages. First, one needs to consider the three primary steps that are performed by the memory BIST: writing the test pattern, reading it and comparing it to the expected result. Pipelining allows these three steps to be executed concurrently. While new data is being written, the results of a previous read are recorded, and a comparison operation on an even earlier read can be done within one clock cycle. This cuts test time by nearly two-thirds. Also, the high rate of operations on the memory can uncover faults that are undetectable with non-pipelined approaches.

A pipelined memory BIST architecture also makes it easier to meet timing requirements when testing very high-speed memories. The increased registration means the length of critical paths in the test circuitry can be decreased. These delay savings mean the additional quality provided by at-speed testing can be applied to a much larger set of embedded memories.

The application of at-speed testing is facilitated by the increased usage of embedded test muxes. Having test muxes designed directly into the memory means the added BIST structures will have minimal impact on the system line delays. Furthermore, embedded-memory providers can optimize the embedded test muxes to reduce the delay impact. It is important that the memory BIST application tool recognize memories with these embedded muxes so they can be utilized without the need for manually modifying the netlist.

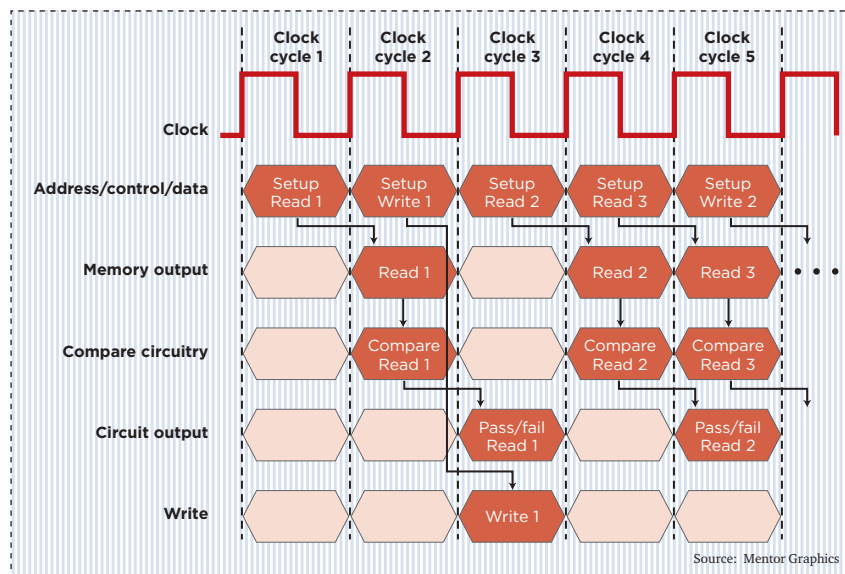
At-speed diagnostics

Just as important as determining which embedded memories are defective is analyzing the cause of the failure. It is becoming much more common for nanometer designs to include diagnosis circuitry in the memory BIST. However, many implementations of diagnostic memory

test circuits may be unable to perform proper at-speed application. Using a relatively slow clock to feed failure data out to the tester during memory fault diagnosis manifests this problem. If multiple faults exist, the BIST must stop and wait for the fault data to download to the tester. If the BIST simply starts again after the data is fed out, the at-speed fault model is defeated and defects can be missed. To correct this problem, the memory BIST must restart the test, go back to an earlier address and skip failures that were previously reported. This allows the BIST to get a running start and ensures that patterns are applied properly for all memory cells, at-speed, during diagnostic analysis.

The combination of a flexible memory BIST engine that allows custom variations to the March algorithm, with enhanced at-speed application, provides the basis for ensuring high-quality testing of SoC designs with hundreds of embedded memories. With the trend toward designs with more memory than logic, memory BIST will become a major contributor to decreasing DPM and improving product quality and yield.

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Memory BIST pipelining technique improves throughput and at-speed testing.