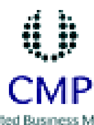

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Test diagnostic tool helps to increase yields

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SANTA CRUZ, Calif. — Pity the IC failure analysis expert. While scan test data provides a starting point for diagnosis, isolating fault locations and identifying defect types is tough. Mentor Graphics Corp. promises to simplify that process this week with the release of its YieldAssist diagnostic tool.

After taking in gate-level netlists, test pattern sets and failure files from manufacturing test, YieldAssist generates reports that identify and classify suspect defect types. Users can view the defects in chip layouts using Mentor's Calibre results viewing environment (RVE). The end result, Mentor claims, is yield improvement, possibly through better design rules that filter back to the IC design environment.

"In manufacturing test, you could have thousands of failures per day, and in the past those just got logged in as failures and got thrown away," said Greg Aldrich, marketing director for Mentor Graphics' test division. "But you can use the scan test data to facilitate diagnostics for the purpose of yield improvement."

The target market for YieldAssist, said Aldrich, is failure analysis groups inside fabs or IDMs. Those groups are charged with identifying failure mechanisms and creating additional tests that will detect them in the future. What they discover about defect types can also be used to improve yields.

Defect types reported
Aldrich cited a customer example in which 30 percent of the failures were found to be caused by the same mechanism: a bridge between signals running over wide metal. The problem was caused by the chemical mechanical polishing process. The customer created a "hard" design rule to avoid the bridging defects in the future.

Further, noted Aldrich, there are an increasing number of "nonvisual" defects. "Things are only failing electrically and are becoming more and more difficult to diagnose through things like in-line inspection," he said.

In addition to bridging defects, YieldAssist can find opens, stuck-at-one and stuck-at-zero shorts, and delay-related defects. It can find two-way and three-way bridges.

YieldAssist takes test pattern data from Mentor's FastScan or TestKompress automatic test pattern generation (ATPG) tools. At this time, it does not work with ATPG tools from other vendors. Aldrich said there has been no decision about working with other ATPG tools in the future. YieldAssist doesn't require Calibre to run, but it does require Calibre in order to view defects in the layout.

After receiving a netlist, test pattern set and failure file, YieldAssist first runs a pattern consistency check to make sure the test patterns match the design. It then runs a failure file consistency check to make sure the failure file matches the test patterns and the design.

Next, the tool maps failures to suspect classifications, such as opens, shorts or bridging. It classifies the suspects and issues a

score for each, indicating how well the suspect behavior matches with the observed failures. YieldAssist reports the defect information, pin path, logical pin name and net name.

Calibre marks the spot

If users brings up Calibre RVE, Aldrich noted, they can view the exact location where signals overlap and can potentially bridge. Aldrich added that YieldAssist diagnoses scan chain failures as well as defects.

Aldrich said that YieldAssist was developed internally at Mentor and that much of it was based on work originally done for the TestKompress ATPG compression product. "One of the goals when we did compression was to make sure we could diagnose things from compressed patterns," he said. "We knew that in the future, we'd need to use test data from manufacturing to help with yield."

YieldAssist is available now starting at $126,000 per year. The product has received an endorsement from Taiwan Semiconductor Manufacturing Co. Ltd.

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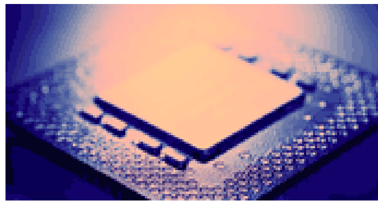

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