



FABLESS FORUM

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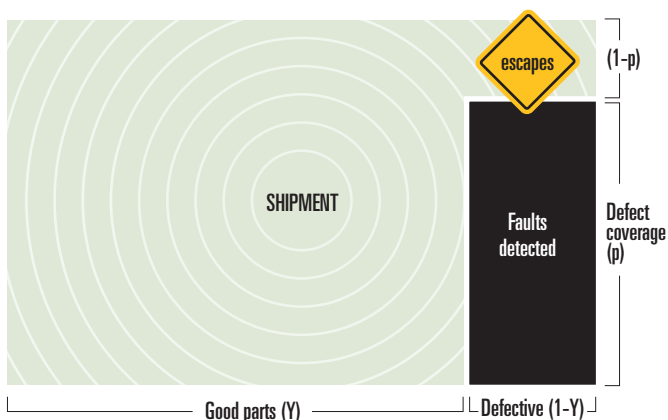
IMPROVING TEST QUALITY AND REDUCING ESCAPES

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When it comes to test, the semiconductor industry is hitting the wall. Scan and the “stuck-at” fault model have been the standard for semiconductor test for more than a decade, but as system-on-chip (SOC) designs move to 0.13-micron processes and below, manufacturing test will undergo significant changes. Standard “stuck-at” tests alone will no longer be sufficient to ensure test quality and target defect rates. To remain competitive and ensure that quality parts are delivered to end customers, semiconductor companies across the board will need to reconsider their test strategies and upgrade their test methodologies.

The relationship between test quality and test escapes is pretty straightforward. Given a specific process technology with a specific yield, the defect coverage (or quality of test) will determine how many defective devices “escape” the manufacturing test process. A lower yield means better tests are needed to ensure low “escape” rates. How much better do they need to be? Given a 90% yield and a 95% defect coverage, the computed defect per million (DPM) rate is 5,254. With an 80% yield, that same 95% defect coverage would result in a DPM rate of over 11,000 — more than double the original rate. To maintain the DPM rate, either the yield must be brought back to 90% or the defect coverage must be dramatically improved, or some combination of both is needed.

Figure 1: Yield, Defect Coverage and Test Escapes



The variable that SOC design groups can influence and control is defect coverage. Defect coverage is a measure of how effective the manufacturing tests are at detecting any possible defect that may occur. Historically, test coverage of single “stuck-at” fault coverage has been the measure used for defect coverage. A “stuck-at” test assumes a hard failure where a given node is shorted (or stuck) to a logic 0 or 1 value. The defect spectrum changes as process technologies move to the sub-nanometer range and this measure is no longer sufficient. The number of resistive defects is growing, and

standard “stuck-at” test vectors do not detect a large portion of these types of defects. These resistive defects manifest themselves as speed-related problems as opposed to hard “stuck-at” failures. To detect these problems, a comprehensive SOC test methodology that includes not only DC tests (such as “stuck-at” patterns) but also AC (or “at-speed”) tests is required. Over the next several years, test methodologies across the board will need to be more effective at screening out speed-related defects to maintain acceptable defect (or DPM) levels.

The importance of “at-speed” test is growing exponentially as process technologies continue to shrink. NVIDIA has extensive experience with at-speed testing and other types of non-static testing. As their SOC designs moved to 0.15-micron processes and below, extensive experiments were done to ensure that the quality of their shipped devices was maintained. NVIDIA noticed a dramatic increase in “at-speed” test fallout as process technology shrunk below 0.18-micron. As the company moved from a 0.18-micron process to 0.15-micron, it experienced an increase in “at-speed” fallout, anywhere from 3x to 5x. These were failing devices that were only detected by the “at-speed” vectors. Had NVIDIA not made a significant investment to ensure high test quality, these devices would have passed through initial screening. Moving to 0.13-micron, another 4x increase in “at-speed” failures was observed. In fact, based on historical data, it appears that the last technology where “stuck-at” DC testing alone is sufficient to ensure reasonable DPM levels is 0.18-micron. Once designs move below 0.18-micron, “at-speed” testing is no longer optional.

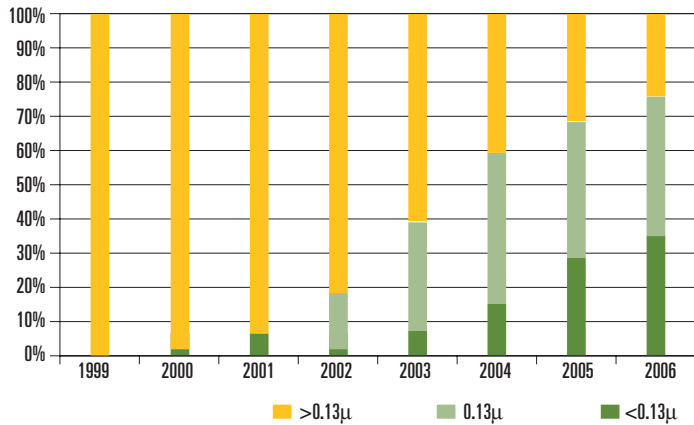
Historically, “at-speed” testing of SOC devices has been done using functional tests where the device is exercised on the tester in the same manner as in the intended application. That means that all access to the device is limited to the IO pins. There are two major drawbacks to this functional approach to “at-speed” test. First, it is often very difficult and time consuming to create functional tests that exercise all of the logic embedded into a 10 million-gate SOC. It is even more difficult to determine what logic was or was not exercised to get any accurate test coverage information for the given set of functional tests. The second major drawback to a functional approach is cost. Since functional patterns are all delivered “at-speed” through the chip’s IO pins, a tester with many high-speed IO pins is necessary. This dramatically increases the cost of the automatic test equipment (ATE) needed since a major factor in ATE cost is the number of high-speed pins required.

As “at-speed” test becomes a requirement, scan-based “transition” patterns are quickly becoming the standard. Transition patterns target the entire design for speed-related defects. Since they target every node in the design for a slow transition, the methodology for creating and applying this type of pattern is very similar to that of “stuck-at” patterns — a methodology in which most SOC manufacturers are already well versed. A transition pattern typically involves several steps:

1. Load the scan chain to set up initial values such that the proper transitions will occur when a clock signal is issued.
2. Issue a “launch” clock sequence that starts the transitions.
3. Issue a “capture” clock sequence that captures the expected values.
4. Unload the scan chain to verify that the expected data was captured.

At-speed testing with transition patterns requires that only the clock signal be high-speed. This can significantly reduce the cost of the tester. Another advantage of this approach is the use of scan to access the internal nodes of the design for structural testing. This means that an accurate measure of the test coverage can be obtained, and that high coverage patterns can be created algorithmically using automatic test pattern generation (ATPG) tools. As SOC clock speeds start to exceed the limits of even high-end test equipment, newer approaches are emerging that allow a design’s own internal clocks to be used to issue the “at-speed” launch and capture clock sequences. These approaches completely eliminate the need for high-speed pins on the test equipment itself.

Figure 2: North America, ASIC Designs by Drawn Line Width (% of Designs)



Source: Gartner, November 2002

Creating more effective tests for larger SOC designs, and testing for more types of defects comes at a cost — increased test data volume and longer test times. At-speed transition testing alone can easily double the pattern volume, compared to static “stuck-at” tests.

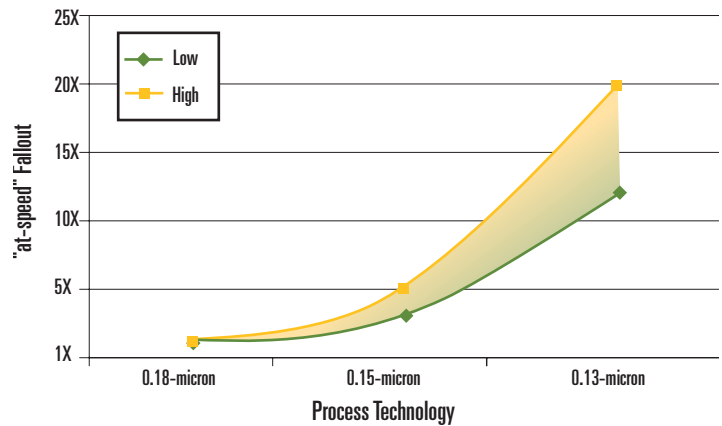
To maintain/improve quality as the company moved to smaller process technologies, one change NVIDIA made to its testing process was the reallocation of wafer sort tester memory. The amount of memory dedicated to “non-stuck-at” structured standard cell test increased to 25%, while the amount of memory allocated to “stuck-at” testing decreased to about 50%. Exploding gate counts are driving up test data volume and test cost even further. Improving test quality while controlling cost will be a key requirement. While much attention has been paid to “reducing the cost of test,” the real struggle that semiconductor manufacturers face as they move to smaller process technologies is one of *controlling the cost of test* while maintaining or improving the quality or effectiveness of the testing they do.

Two major factors contribute to the cost of test — the capital cost of the test equipment itself and the amount of time required to test each device. With a structural approach to “at-speed” test, capital equipment costs can be reduced since fewer high-speed channels are required. The amount of test time, however, must also be controlled to control the rising cost of high-quality testing.

With a deterministic scan-based test, the test time is directly proportional to the amount of test data that must be loaded/unloaded and the

number of scan channels available to do the loading. To significantly reduce the amount of test data required, and therefore, the test time, approaches that utilize on-chip decompression and compression hardware will be required. Utilizing these new techniques, highly compressed pattern sets (up to 100x smaller than the original size of the test set) are created. These highly compressed test sets are then delivered to the device from the tester just as they are with traditional scan patterns today. The difference is that the on-chip decompressor takes the highly compressed pattern and expands it to a fully specified pattern and delivers it through a large number of internal scan channels. Once the pattern is delivered and the responses are captured, another on-chip compactor compresses the response as it is shifted back out to the tester. Using this embedded deterministic test approach, the amount of test data and test time can be reduced by up to a factor of 100, making it much more cost effective to add additional tests to improve test quality. An added benefit is that this embedded approach does not require changes to the functional (or core) portion of the design. The decompression and compaction logic

Figure 3: Increase in “At-Speed” Defects as Process Size Shrinks



Source: NVIDIA

are added outside the core design and are only inserted into the scan path during test mode. Sequential “at-speed” patterns can be created and delivered just like regular scan patterns, and since it is still a deterministic approach, no additional logic, such as test points or x-bounding, needs to be added to guarantee high coverage.

High-quality manufacturing test will become even more critical as process technologies continue to shrink. The need for “at-speed” testing has become a must as processes reach 0.13-micron and below. As process technology shrinks even further, other types of tests, such as multiple detect patterns that target bridging and other unmodeled defects, will also become necessary. Ultimately, to control costs while dealing with this mountain of test data, embedded compression will become the standard for SOC design. ■

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