DFT Approaches Enable Mass Production Test

Ron Press & Takeo Kobayashi
Mentor Graphics Corporation

Speaker Biography

Ron Press is the technical marketing manager of the design for test products at Mentor Graphics Corp. The 20-year veteran of the test and DFT industry has presented seminars on DFT and test throughout the world. Mr. Press co-authored a patent on clock switching and reduced pin count testing. Ron has published many papers in the field of test and is a member of the ITC Steering Committee.

Abstract

Test compression technology was adopted to enable additional scan patterns to be applied without changing the test interface. However, test compression and test approaches can also be used to reduce the ATE (automatic test equipment) and tester interface requirements. As a result, not only can existing testers be used to apply additional tests, the test interface can be reduced to a very small amount of serial channels. This eases the adoption of multi-site testing, thereby increasing test throughput and mass volume production. In addition, the compressed fail values of each device can be directly used for diagnostics, enabling a software approach to failure and yield analysis. Three industry designs are used to demonstrate high levels of compression with one or two serial channels. Results are shown in terms of improved test quality, test compression, and diagnostics while reducing the test interface for a mass production environment.

Battling Increasing Test Requirements

Whilst the economics of production test push for more tester throughput, quality goals are demanding more tests.

Scan test is a standard methodology for almost all large digital devices with volume production. Automatic test pattern generation (ATPG) is facilitated by scan technology for even the most complex devices. With scan, every sequential gate is serially connected as a series of shift registers during test mode - referred to as scan chains. As a result, each pattern serially loads the scan chains to place the entire circuit in a desired state. Next, the circuit is clocked and the functional response is captured. Finally, the circuit is again placed into shift mode to shift out the response for comparison.

Moore’s law predicts that gate counts increase by roughly four times every three years [1]. Growth in gate count will increase the cycles and data per test pattern to at least the same rate. Thus, test time increases by a minimum of four times every three years since each scan chain grows four times longer.

The same advances in silicon fabrication that enable increased gate counts also cause a change in the nature of defects that occur. As a result, the basic scan patterns that were sufficient for many companies five years ago need to be

supplemented with other scan patterns. For example, devices produced with 130 nm or smaller fabrication processes often have a population of timing defects greater than 2%. Consequently, at-speed transition scan testing is mandatory in many production test environments.

Additional tests are growing in popularity to further improve test quality and reduce defective parts from being shipped. Several example of the newer scan test methods are multiple-detect [2], timing-aware [3], open, and deterministic bridge patterns.

Growing device gate counts and at-speed transition patterns can increase the device test time by a huge amount. This pattern growth is necessary just to maintain defects per million (DPM) levels as companies move to smaller technology nodes. Furthermore, any additional newer scan tests used to improve test quality or to deal with defects in new fabrication processes will grow the test time even more. Applying these tests can quickly exceed tester capacity if a solution isn't found.

Fortunately, compression technologies have been introduced to reduce the time and data to apply scan test patterns by as much as 100 times [4]. As a result, the additional tests can be applied without negatively impacting tester throughput.

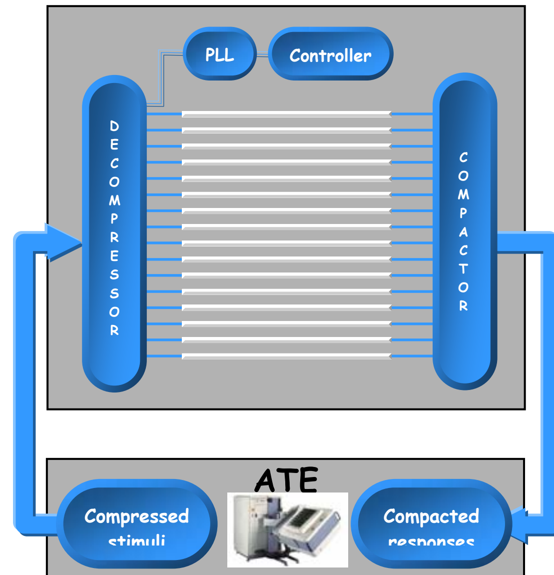

Figure 1. EDT (embedded deterministic test) applies tests 100x faster using the same tester scan channels

Options to Increase Production Test Throughput

Production test throughput directly impacts a product's cost. In recent years, there has been growing concern that the cost of test is increasing to the point that it is becoming larger than the cost to manufacture the device. Testers are a significant capital expense and need to be used as efficiently as possible.

It is advantageous to increase tester throughput to distribute the cost of the tester over many more devices tested on it per day. Several options exist that can increase tester throughput

- Reduce the amount of testing – this is not a reasonable approach for most products. The reduced test correlates to more defective parts escaping, thereby decreasing product quality.
- Improve test efficiency – apply the same or equivalent tests in less time than is done today.

This is possible using test compression.
- Multi-site testing - test multiple devices in parallel.

Controlling Costs

Multi-site testing is used in volume production environments to drive the test costs down. This test approach can significantly improve tester throughput and reduce costs [5]. Multiple devices are tested in parallel within the same time it would normally take to test one device. Additionally, there is a cost savings by only needing one insertion for multiple devices instead of one insertion per device.

It is more common to test more devices in parallel during wafer test than during packaged device test. Often a few escapes from wafer test are acceptable as long as the majority of defective parts can be identified. As a result, some companies are testing over 200 devices in parallel during wafer test. This is a potential 200x improvement in tester throughput. Packaged devices often require more pin contact for IO parametric tests. So, even though multi-site testing is used on packages devices it is often in the range of 10 devices instead of hundreds.

Cost tradeoffs can get complicated when trying to determine the best multi-site configuration for test [6]. There is a delicate balance between tester channels, device pins, and tester memory.

Reducing the ATE Interface

Each tester pin and interface to a device being tested has an associated cost with it. It is advantageous to reduce the tester/device interface to as few pins as possible. Not only are there costs related to load boards and tester channels but the test is also more reliable with fewer pins. The risk of a bad contact grows with each contact point.

Many reduced pin count test (RPCT) approaches have been proposed to provide pseudo pin access without physically contacting each pin. Boundary scan can be used to access the boundary scan registers for control and observability close to each IO pin. One approach configures the boundary scan registers as scan cells during scan testing while avoiding propagation of unknown states during at-speed test [7].

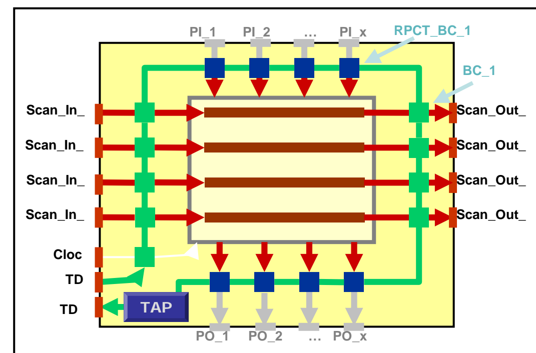

Figure 2. Reduced pin count test

A scan compression technology such as EDT (embedded deterministic test) solves the issue of applying more patterns for growing designs without increasing test time. However, the technology also can be used to reduce the number of scan channels connected to a tester. For example, instead of using EDT to make a 16 scan channel interface load patterns faster, some of the compression can be used to reduce the tester interface. Thus, part of the compression capability can reduce the interface to two scan channels while still applying each pattern 10 times faster.

Many compression techniques lose their effectiveness when trying to operate with very few tester scan channels. The existence of X-states (unknown values) that can appear due to false paths during at-speed testing, can disrupt test coverage and compression. X-masking within the compression technology can maintain the test coverage. However, most masking approaches end up requiring more data to define the masks or they block many observe states when operating. Both cases result in significantly reduced compression in the presence of X-states, especially if only using one or two tester scan channels. A recent technology called Xpress works with EDT to mask X-states with software optimized mask selection [8]. The software optimization results in much higher compression in the presence of X-states.

Use Volume Failure Diagnostics to Improve Yield

Multi-site testing can greatly improve tester throughput and test many devices in the time it would normally take to test one device. Mass volume production is also dependent on establishing an acceptable yield and identifying yield limiting factors. A minimum yield must be established before volume production can start. When the initial yield is low then there is a critical delay in bringing the product to market. Scan failure diagnostics is a quick method of identifying and locating defects [9]. Scan failing data from a tester can be analyzed through pattern analysis, identifying the root cause defect type. The physical database is linked to the scan diagnostics tool such that not only is the defect reported but the physical location identified as well. Hence, a quick software analysis can direct failure analysis engineers to the defect type and location. They can use this information to determine how to resolve the issue in the fabrication process or physical device design.

During volume production the scan diagnostics must work directly with the fail data coming from the tester. Much of the volume production has moved to compression technology. Fortunately, scan diagnostics can work directly with the compressed pattern responses from the tester, avoiding off-line re-test [10].

Subtle changes in the yield of mass production devices can have a huge effect on the production costs. Thus, it is vital not only to bring the yield to an acceptable level initially but also to continuously monitor and improve the yield. Many volume production environments mark devices as defective at the first sign of a failure and discard them. Now with the advent of volume scan diagnostics, fail data can be automatically sent from the tester to a server [11]. Volume scan diagnostics tools perform volume analysis as background operations. Thus, at any instance of time the volume production diagnostics results can be checked for defect trends.

Mass volume production will often use multi-site testing with the potential to detect many failures in one multi-site insertion. The volume scan diagnostics can deal with varying fail file data by automatically distributing the diagnostics over many diagnostics analyzers. Testers just need to send the fail data to the central server location.

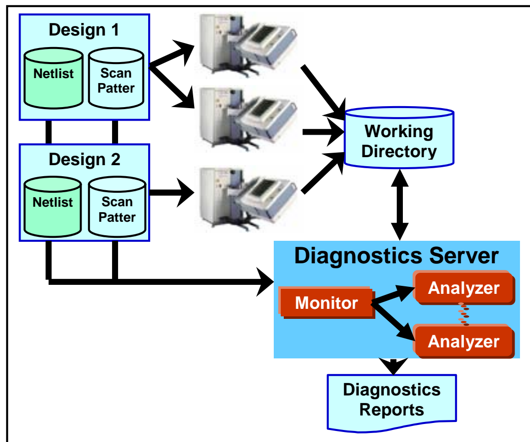

Figure 3. Volume diagnostics environment

Test patterns can be broadcast to multiple devices from common tester channels to apply a multi-site test pattern. However, to identify the individual failing devices, each device will need dedicated tester channels for observation and verification.

One new approach to fail detection for multi-site test is to broadcast the expected data from the tester to all devices. Then the devices can internally compare to captured scan response. Though this is not a common practice today, it has potential to significantly reduce the tester interface.

Case Study

Mass production multi-site testing can be facilitated by using just one or two tester channels. Three industry designs are used to demonstrate the ability to perform test compression using one or two tester channels. These same designs are used to show the effectiveness of scan diagnostics at these aggressive compression rates with minimal scan IO. Table 1 shows the properties of the design and compression configurations.

Experiments were performed comparing a baseline of bypass mode uncompressed patterns to compressed patterns. Bypass patterns directly connect to the internal scan chains and circumvent the EDT compression logic. All experiments are based on achieving the maximum coverage. In design A, the bypass patterns are configured with 524 scan chains as if they were directly controlled and observed. Then EDT compression is configured with only 2 tester channels connected to the device. The bypass patterns and EDT compression are based on the standard operation of EDT software.

Next, a new version of EDT with Xpress technology was used. This version has more effective X-masking as well as new software compression to reduce the overall pattern count. Table 2 shows the results. By using two channels with the new version of EDT with Xpress, the test data volume is reduced by 131x.

It is unrealistic to assume 524 tester channels are available to provide a scan test. For this case, if 32 tester channels were used for device A bypass scan test then each scan chain would be roughly 4000 scan cells long. The test coverage and number of patterns are consistent with any number of scan channels for bypass configurations. The bypass results with 32 tester channels would take 19.6M tester cycles to apply the tests (4.9K patterns x 4000 cycles/pattern). At 50 MHz, this would take 0.39 seconds to perform the test. However, with EDT Xpress compression, the tester cycles per pattern is roughly 265 (127K/524).

In this case, it took 8.5K patterns to reach the same maximum coverage as

bypass patterns. Thus, EDT Xpress takes 2.5M cycles and 0.045 seconds to apply the tests. So, in the case of design A, the tester scan channels can be reduced from 32 to 2 (16x) while also reducing the test time by about 8x. In addition, the test compression can be used to apply supplemental tests such as multiple detect patterns which are shown at the bottom of Table 2. Similarly, Table 3 shows transition pattern results for design B and includes results for timing-aware additional patterns.

In design C, the average number of X-states per pattern is more than 6%. Other compression approaches have great difficultly with such a high population of X-states. Previous EDT technology results in 122K patterns because a significant amount of masking is necessary to ensure the maximum test coverage with only one scan channel. However, the new software-optimized Xpress produces roughly an order of magnitude fewer patterns and 92x compression.

Scan diagnostics was performed on the same industry designs to compare the direct bypass diagnostics results with one or two channel compression. Fail values were simulated inside the designs to produce bypass and compressed pattern fail results. These emulate what the tester would report as fail values if these defects existed in devices being tested. Table 5 shows the results for these extreme levels of compression. The data shown is the number of scan diagnostics suspects with a score of 100. The number in parentheses represents additional suspects that have some ambiguity and lower confidence of being the defect. Notice that with only a few fail cycles, the one or two channel compression does not perform as well as bypass patterns. However, with 7 to 10 fail cycles the resolution of EDT Xpress scan diagnostics is just as good as bypass pattern diagnostics.

Conclusion

Mass volume production necessitates reduced pins and test application times. With the advent of aggressive compression using one or two channels, complex tradeoffs can be avoided because the small channel interface per device can exist while still reducing test time. A case study shows that a design with 32 scan channels can be reduced to only two channels for multi-site test while still reducing the test time significantly. Thus, additional test types can be added to improve the test quality and lower DPM while still improving throughput. In addition, tester fail data from the compressed patterns produces the same resolution to one defect as direct access to scan chains. With high levels of multi-site testing and automated volume scan diagnostics, mass volume production can be supported.

References

1. G. E. Moore, “Cramming more components onto integrated circuits”, Electronics, Volume 38, Number 8, April 19, 1965.
2. B. Benware, et. al., “Impact of Multiple-Detect Test Patterns on Product Quality”, Proc. ITC 2003, pp. 1031-1040.
3. X. Lin, et. al., “Timing-Aware ATPG: A Novel Test Generation Method for High-Quality At-speed Test”, Asian Test Symposium 2006

4. J. Rajski, et al., “Embedded Deterministic Test for Low Cost Manufacturing Test,” Proc. Int’l Test Conf. (ITC 02), IEEE Press, 2002, pp. 301-310.
5. L. Boon, “Test Cost Saving and Challenges in the Implementation of x6 and x8 Parallel Testing on Freescale 16-bit HCS12 Micro-controller Product Family”, Proc, IEEE Workship on Electronic Design, Test and Applications (DELTA’06), 2005.
6. S. Goel, et. al., “On-Chip Test Infrastructure Design for Optimal Multi-Site Testing of System Chips”, Proc, DATE 2005.
7. J. Jahangiri, et. al., “Achieving High Test Quality with Reduced Pin Count Testing,” ATS 2005.
8. R. Press, “Embedded Compression for Production Test”, Evaluation Engineering, October 2007.
9. J. Mekkoth, et. al., “Yield Learning with Layout-aware Advanced Scan Diagnosis”, Proc. International Symposium for Testing and Failure Analysis (ISTFA), Nov. 2006.
10. Y. Huang, et. al., “Compressed Pattern Diagnosis For Scan Chain Failures”, Proc. Int’l Test Conf. (ITC 05), IEEE Press, 2005.
11. H. Tang, et. al., “Analyzing Volume Diagnosis Results with Statistical Learning for Yield Improvement”, IEEE European Test Symposium (ETS'07) 2007.

Table 1. Scan designs for case study

Design	Gates	Scan cells	# chains	# channels	Pattern type
A	1.9M	127K	524	2	Stuck-at
B	6.5M	513K	112	1	Transition
C	2.4M	156K	128	1	Transition

Table 2. Design A compression results (X-states average 0.37% per pattern)

	Patterns	Data volume	Compression
Bypass	4.9K	662M	1x
EDT	35.3K	19.6M	34x
Xpress	8.5K	5M	131x
3-detect Xpress	*31.5K*	*17M*	*37X*

Table 3. Design B compression results (X-states average 0.35% per pattern)

	Patterns	Data volume	Compression
Bypass	28.5K	14G	1x
EDT	97.2K	449M	33x
Xpress	32K	148M	98x
Timing-aware ATPG (Xpress)	*98K*	*456M*	*32x*

Table 4. Design C compression results (X-states average 6.7% per pattern)

	Patterns	Data volume	Compression
Bypass	12K	2G	1x
EDT	122K	154M	13x
Xpress	16.9K	21M	92x

Table 5. Compressed pattern scan diagnostics high confidence suspects (lower confidence suspects in parentheses)

	1st 5 fail cycles		1st 7 fail cycles		1st 10 fail cycles		1st 16 fail cycles	
	Bypass	Xpress	Bypass	Xpress	Bypass	Xpress	Bypass	Xpress
Design A	2 (7)	5 (432)	1 (4)	1 (50)	1 (3)	1 (4)	1 (3)	1 (3)
Design B	1 (9)	2 (16)	1 (9)	2 (12)	1 (9)	1 (9)	1 (9)	1 (9)