

**A P P N O T E S <sup>SM</sup>****MAJIC® Interface Specifications for ARM Debug  
Interface and Intel XScale® Technology  
(MAJIC-MT, MAJIC-LX, MAJIC-LT, MAJICO)**

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**Introduction**

This application note provides technical specifications for the MAJIC® Series of Intelligent Debug Probes when used with ARM processors that include the ARM Debug Macrocell, or with processors based on Intel XScale® technology. It includes information on the following:

- Cabling options.
- Debug connector details: pin-outs and recommended part numbers.
- Board design considerations.
- Electrical specifications for the MAJIC-MT, MAJIC-LX, and MAJIC-LT, and MAJICO models. For information on older probe models, please contact technical support.

## Cable Kit Options

There are several cable kit options available for the MAJIC series, and it is important to choose the right cable kit(s) for your target board(s).

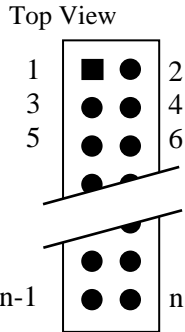
The following table shows the most commonly used cable kits for target boards incorporating an ARM core or Intel XScale® core. Details on the connectors' pin-outs, and recommended board design practices are described on the following pages.

Target Connector	Cable Kit
12-Pin Fine Pitch JTAG	CK-FPJ12
14-Pin JTAG, Texas Instruments pin assignment	CK-TX14
14-Pin JTAG, ARM pin assignment	CK-ARM14
20-Pin JTAG, ARM pin assignment	CK-ARM20
20-Pin JTAG, ARM pin-out and <u>separate</u> 38-Pin Mictor for ETM	CK-ARM20
38-Pin Mictor, <u>combined</u> JTAG and ETM	CK-ARM38

### NOTE:

- These connectors are the most common, but MAJIC supports many others as well. If the connector you have does not match the JTAG Header pin-out options shown in the following table. Please contact technical support for more information.
- If you are trying to decide which connector to use on your own hardware design, and do not need ARM/ETM support, then Mentor Graphics recommends either the ARM20 for ease of use, or the FPJ12 for small form factor applications which do not require RTCK.
- The CK-ARM38 cable only supports the JTAG signals; all ETM signals are left unconnected.

## JTAG Headers



### NOTE:

- The ARM14 and FPJ12 connectors are **not** suitable for ARM processors that require the RTCLK signal.
- Technical details on the JTAG signals are discussed in the *Board Design Considerations* and *Electrical Specifications* sections of this application note.
- See [Debug Connector Part Numbers](#) for recommended connector vendor part numbers.
- Pull-up and series termination resistors should be placed near the CPU pins.

Pin	ARM 20-Pin 2x10 0.10"		ARM 14-Pin 2x7 0.10"		TX 14-Pin 2x7 0.10"		FPJ 12-Pin 2x6 0.05"		
	Signal	Termination	Signal	Termination	Signal	Termination	Signal	Termination	
1	VTRef	10k pull-up	VTRef	10k pull-up	TMS	10k pull-up	nTRST	10k pull-up	
2	VSupply	(not used)	GND		nTRST	10k pull-up	GND		
3	nTRST	10k pull-up	nTRST	10k pull-up	TDI	10k pull-up	TDI	10k pull-up	
4	GND		GND		GND		GND		
5	TDI	10k pull-up	TDI	10k pull-up	VTRef	10k pull-up	TDO	33 Ω series	
6	GND		GND		n/c		GND		
7	TMS	10k pull-up	TMS	10k pull-up	TDO	33 Ω series	TMS	10k pull-up	
8	GND		GND		GND		GND		
9	TCK	10k pull-up	TCK	10k pull-up	RTCK	33 Ω series	TCK	10k pull-up	
10	GND		GND		GND		GND		
11	RTCK	33 Ω series	TDO	33 Ω series	TCK	10k pull-up	nSRST	10k pull-up	
12	GND		nSRST	10k pull-up	GND		GND		
13	TDO	33 Ω series	VTRef	10k pull-up	nEMU0	(not used)			
14	GND		GND		nEMU1	(not used)			
15	nSRST	10k pull-up							
16	GND								
17	DBGQRQ	10k pull-down (not used)							
18	GND								
19	DBGACK	10k pull-down (not used)							
20	GND								

### Debug Connector Part Numbers

Connector	Part Number	Description
12-pin, fine pitch header	Samtec FTSH-106-01-F-DV-A	Dual row (2x6), 0.05 inch spacing, surface mount header
14-pin header	3M 2414-600UB	Dual row (2x7), 0.1 inch spacing, surface mount header
20-pin header	3M 2520-6002UB	Dual row (2x10), 0.1 inch spacing, surface mount header
38-pin Mictor	AMP 2-767004-2	Vertical, surface mount, board to board/cable connector
38-pin Mictor	AMP 767054-1	Vertical, surface mount, board to board/cable connector
38-pin Mictor	AMP 767061-1	Vertical, surface mount, board to board/cable connector
38-pin Mictor	AMP 767044-1	Right Angle, straddle mount, board to board/cable connector

**NOTE:** Refer to the connector vendor's technical documentation for dimensions and other PCB layout details.

## Board Design Considerations

This section provides additional information on board design considerations that arise when designing a target board that incorporates an ARM core or Intel XScale processor.

### Reset Management

- The nSRST (system reset) signal should be connected so that the target system (including the CPU) will be reset when it is asserted (low) by the MAJIC® probe, but will **not** result in nTRST (JTAG reset) being asserted at the target processor. This is recommended for ARM targets, and is required for full support with Intel XScale® cores.
- The nSRST signal is an open-collector signal, so you must provide a pull-up for this signal. It may be tied directly to the reset switch or power-up reset circuit on your board (unless that results in TRST\* being asserted as well).

### JTAG Interface

- Some CPU data sheets recommend a pull-down on certain JTAG signals instead of a pull-up. The MAJIC® probe can support that recommendation as long as at least one of nSRST, nTRST, or VREF is pulled up, but the signals should not be left floating.
- Not all CPU variants provide an RTCK signal. If your CPU does not have this signal, then the RTCK pin on the debug connector should be grounded or pulled up with a 10k resistor. Mentor Graphics strongly recommends against connecting TCK directly to RTCK, as this effectively doubles the length of the TCK signal, and puts your CPU in the middle of the TCK net, which drastically reduces the maximum JTAG clock rate that can be supported for such a board.
- If you have more than one processor that supports RTCK, then RTCK from the processor with the slowest system clock should be used. Alternatively, you can daisy chain RTCK from one device to TCK of the next device, following the same path as TDO-TDI. The best solution, however, is to combine the RTCK signal from all of the cores into one RTCK signal that is presented to the MAJIC® probe. Please contact technical support for additional information.

### PCB Layout

- Avoid placing any tall components near the debug connector, and locate it in a way that is easy to reach (near the edge of the board). We recommend clearly labeling the debug connector and the position of pin 1 on the PCB.
- If you have more than one JTAG device on the scan chain, then the debug connector should be at the end of the JTAG nets, not in the center of the nets (i.e. the JTAG signals must not fan out from the debug connector to multiple devices). Please refer to the *MAJIC Support for Multi-TAP JTAG Configurations* application note for additional information.

## Electrical Characteristics

The following tables provide electrical characteristics for the JTAG interface.

DC Characteristics	Note	Specification
Target I/O Voltage		1.2v to 3.3v (nominal)
Output Drive: TCK, nTRST, TMS, TDI		± 2mA at 1.2v ± 6mA at 1.8V ± 18mA at 2.5V ± 24mA at 3.3V
Output Drive: nSRST	1.1	+2mA at 1.2v, -120µA at 1.2v +6mA, -180µA at 1.8v +8mA, -250µA at 2.5v +16mA, -330µA at 3.3v
Input Loading: TDO, RTCLK		45pF to ground 10k pull-up to I/O voltage

AC Characteristics	Note	Specification
Max TCK Frequency (75pF load)	1.2 1.3	40MHz at 3.3v 20MHz at 1.8v 10MHz at 1.2v
TCK Duty Cycle		40/60% to 60/40%

### NOTE:

- 1.1: nSRST is a pseudo-open-collector output, with a 10k pull-up to the I/O voltage level.
- 1.2: Maximum frequency is a function of the I/O voltage level vs. capacitive loading. Therefore, the maximum supported frequency may be constrained on low voltage targets, and targets with heavily loaded JTAG pins. The MAJIC® probe's TCK frequency is programmable, from <1 to 40MHz.
- 1.3 This specification does not take the target CPU or board design into account. The CPU or target board may not support the full frequency supported by the MAJIC probe.