

**A P P N O T E S<sup>SM</sup>****MAJIC® Interface Specifications for MIPS EJTAG  
(MAJIC-MT, MAJIC-LX, MAJIC-LT, MAJICO)**

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**Introduction**

This application note provides technical specifications for the MAJIC® Series of Intelligent Debug Probes when used with processors that support the MIPS EJTAG debug interface.

- Cabling options.
- Debug connector details: pin-outs and recommended part numbers.
- Board design considerations.
- Electrical specifications for the MAJIC-MT, MAJIC-LX, MAJIC-LT, and MAJICO models.  
For information on older probe models, please contact technical support.

## Cable Kit Options

There are several cable kit options available for the MAJIC series, and it is important to choose the right cable kit(s) for your target board(s).

The following table shows the most commonly used cable kits for target boards incorporating a MIPS processor with an EJTAG debug interface. Details on the connectors' pin-outs, and recommended board design practices follow on the next few pages.

Target Connector	Cable Kit
10-Pin 0.1" IEEE standard JTAG	CK-J10
12-Pin 0.1" IEEE standard JTAG plus RST*	CK-J12
14-Pin 0.1" EJTAG v2.5 (and later)	CK-MIPS14
12-Pin 0.05" EJTAG v2.0	CK-EJ12
20-Pin 0.05" EJTAG v2.0	CK-EJ20
24-Pin 0.05" IDT RC323xx	CK-IDT24
52-Pin 0.05" EJTAG v2.0	CK-EJ52

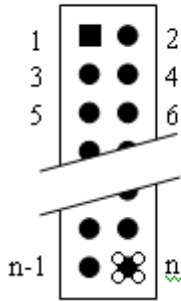
### NOTE:

- The connectors listed are the most common, but MAJIC supports many others as well. If the connector you have does not match the JTAG Header pin-out options shown in the following table, please contact technical support for more information.
- If you are trying to decide which connector to use on your own hardware design, we recommend either the MIPS14 for ease of use, or the EJ12 for small form factor applications.
- The CK-EJxx and CK\_IDT24 cables only support the JTAG signals; all PCTrace signals are left unconnected.

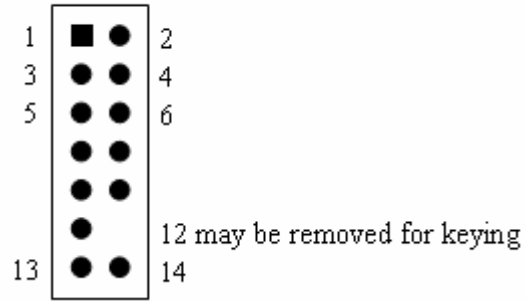
### JTAG Headers

- EJTAG specification v1.5.3 and v2.0 call for dual row male headers with 0.05"x0.05" spacing. The recommended connector is the Samtec FTSH-1xx-01-F-DV-A connector series.
- EJTAG v2.5 and later calls for a 14-pin dual row male header with 0.1"x0.1" spacing. The recommended connector is the 3M part number 2414-600UB.

Top View



Top View



**NOTE:** The debug connector pin-outs and recommended connection are shown in the following table. Additional technical details on the JTAG signals are discussed in the [Board Design Considerations](#) and [Electrical Characteristics](#) sections of this application note.

### Pin-out and Connection Notes

Pin	CK_EJxx 0.05" Spacing		CK_IDT24 0.05" Spacing	
1	TRST*	10k pull-up	TRST*	10k pull-up
3	TDI/DINT*	10k pull-up	TDI/DINT*	10k pull-up
5	TDO/TPC	33 Ω series	TDO/TPC	33 Ω series
7	TMS	10k pull-up	TMS	10k pull-up
9	TCK	10k pull-up	TCK	10k pull-up
11	RST*	10k pull-up	RST*	10k pull-up
13	PCST[0]	33 Ω series	PCST[0]	33 Ω series
15	PCST[1]	33 Ω series	PCST[1]	33 Ω series
17	PCST[2]	33 Ω series	PCST[2]	33 Ω series
19	DCLK	33 Ω series	DCLK	33 Ω series
21	TPC[2]	33 Ω series	DebugBoot	10k pull-down
23	PCST2[0]	33 Ω series	VIO	10k pull-up
25	PCST2[1]	33 Ω series		
27	PCST2[2]	33 Ω series		
29	TPC[3]	33 Ω series		
31	PCST3[0]	33 Ω series		
33	PCST3[1]	33 Ω series		
35	PCST3[2]	33 Ω series		
37	TPC[4]	33 Ω series		
39	PCST4[0]	33 Ω series		
41	PCST4[1]	33 Ω series		
43	PCST4[2]	33 Ω series		
45	TPC[5]	33 Ω series		
47	TPC[6]	33 Ω series		
49	TPC[7]	33 Ω series		
51	TPC[8]	33 Ω series		
All even numbered pins should be flashed to the ground plane.				

Pin	CK_MIPS14 0.10" Spacing	
1	TRST*	10k pull-up
2	GND	
3	TDI	10k pull-up
4	GND	
5	TDO	33 Ω series
6	GND	
7	TMS	10k pull-up
8	GND	
9	TCK	10k pull-up
10	GND	
11	RST*	10k pull-up
12	Key	(no pin)
13	DINT	10k pull-down
14	VIO	10k pull-up

**NOTE:**

- CK\_J10 is the IEEE standard JTAG connector. Pins 1-10 are wired as with MIPS14 pins 1-10.
- CK\_J12 adds RST\* on pin 11 as with MIPS14 pin 11.
- CK\_EJxx and CK\_IDT24 cables leave all PCST, TPC, and DCLK pins disconnected. Those signals are only supported by the MAJIC-PLUS CKP cables.
- Pull-up and series termination resistors should be placed near the CPU pins.

## Board Design Considerations

This section provides additional information on board design considerations that arise when designing a target board that incorporates a MIPS processor with EJTAG debug interface.

### Reset Management

- The RST\* signal should be connected so that the target system (including the CPU) will be reset when it is asserted (low) by the MAJIC probe, but will **not** result in TRST\* (JTAG reset) being asserted on the target processor. This allows the MAJIC probe to reset the target system upon your command. When both cold and warm resets are provided, warm reset is recommended. This is an optional feature, but RST\* should be pulled up to the target's I/O voltage regardless of whether the reset feature is implemented.
- The RST\* signal is an open-collector signal, so you must provide a pull-up for this signal. It may be tied directly to the reset switch or power-up reset circuit on your board (unless that results in TRST\* being asserted as well).

### JTAG Interface

- The TRST\* signal connection to the processor is optional, but it is recommended that the connector pin be pulled up irrespective of whether it is connected to the processor. It is acceptable to pull down the TRST\* pin, providing that you configure the MAJIC probe to enable its TRST\* output driver (which is the default). In this case, however, you will not be able to use TRST\* for sensing the target power level.
- Some CPU data sheets recommend a pull-down on certain JTAG signals instead of a pull-up. The MAJIC® probe can support that recommendation, but the signals should not be left floating.

### PCB Layout

- Avoid placing any tall components near the EJTAG connector, and locate it in a way that is easy to reach (near the edge of the board). We recommend clearly labeling the EJTAG connector and the position of pin 1 on the PCB.
- If you have more than one JTAG device on the scan chain, then the debug connector should be at the end of the JTAG nets, not in the center of the nets (i.e. the JTAG signals must not fan out from the debug connector to multiple devices). Please refer to the *MAJIC Support for Multi-TAP JTAG Configurations* application note for additional information, especially if your target supports PCTrace.

## Electrical Characteristics

The following tables provide the electrical characteristics for the JTAG interface.

DC Characteristics	Note	Specification
Target I/O Voltage		1.2v to 3.3v (nominal)
Output Drive: TCK, TRST*, TMS, TDI		± 2mA at 1.2v ± 6mA at 1.8V ± 18mA at 2.5V ± 24mA at 3.3V
Output Drive: RST*	1.1	+2mA at 1.2v, -120µA at 1.2v +6mA, -180µA at 1.8v +8mA, -250µA at 2.5v +16mA, -330µA at 3.3v
Input Loading: TDO		45pF to ground 10k pull-up to I/O voltage

AC Characteristics	Note	Specification
Max TCK Frequency (75pF load)	1.2 1.3	40MHz at 3.3v 25MHz at 1.8v 12MHz at 1.2v
TCK Duty Cycle		40/60% to 60/40%

### NOTE:

- 1.1: RST\* is a pseudo-open-collector output, with a 10k pull-up to the I/O voltage level.
- 1.2: Maximum frequency is a function of the I/O voltage level vs. capacitive loading. Therefore, the maximum supported frequency may be constrained on low voltage targets, and targets with heavily loaded JTAG pins. The MAJIC® probe's TCK frequency is programmable, from <1 to 40MHz.
- 1.3 This specification does not take the target CPU or board design into account. The CPU or target board may not support the full frequency supported by the MAJIC probe.