

Questa 6.4 Series Product Comparison			
Feature	ModelSim SE	Questa SV	Questa AFV
	<i>Large Block/System Simulation</i>	<i>Advanced Verification, SystemVerilog</i>	<i>Advanced Verification, All Languages</i>
General			
Licensing - Floating License	■	■	■
Language Neutral License	Option	N/A	N/A
ASIC Sign-Off	■	■	■
Platform-Independent Compiled Database	■	■	■
Native-Compiled Architecture	■	■	■
Incremental Compilation	■	■	■
32/64-Bit Cross-Compatibility	■	■	■
Languages			
SystemVerilog IEEE1800 Design	■	■	■
SystemVerilog IEEE1800 Verification		■	■
VHDL	■	■	■
Verilog	■	■	■
SystemC 2.2 IEEE 1666/OSCI 2.2	Option	Option	■
Mixed Language	Option		■
PSL IEEE 1850			■
Unified Power Format		■	■
Analog/Mixed Signal (Advance MS Product)	Option	Option	Option
Advanced Verification			
Assertion-Based Verification		■	■
Questa Verification Library (Assertion Checker & Monitor Library)		■	■
Constrained-Random Test Generation		■	■
Open Verification Methodology (OVM)		■	■
Codelink (Processor-Based Verification)		Option	Option
Multi-View Verification Components (Verification IP Library)		Option	Option
Verification Management & Coverage			
Code Coverage (with Toggle Coverage)	■	■	■
Functional Coverage		■	■
Unified Coverage DataBase (UCDB)	Code Coverage Only	■	■
Coverage Viewer	Code Coverage Only	■	■
Test Ranking	Code Coverage Only	■	■
Test Plan Tracking		■	■
Design Entry, Debug, and Analysis			
HDL Editor	■	■	■
Integrated Project Manager	■	■	■
Source Code Templates and Wizards	■	■	■
Interactive & Post-Simulation Debug	■	■	■
Dataflow Graphical & Textual Causality Traceback	■	■	■
FSM Debug	■	■	■
Source Annotation	■	■	■
Class Browser		■	■
Dynamic Thread Debug & Control		■	■
OVM-Aware Debugging		■	■
C Debugger	Option ¹	Option ¹	■
Memory Window	■	■	■
Multiple Waveform Windows	■	■	■
Extra Standalone Viewer	Option	Option	Option
Waveform Compare	■	■	■
Transaction Viewing and Analysis	Option ¹	■	■
Protocol Recognition		Option ²	Option ²
JobSpy	■	■	■
SignalSpy	■	■	■
User-Customizable GUI (via Tk)	■	■	■
Simulation			
Single-Kernel Simulation Engine	■	■	■
Verilog RTL & Gate Performance Optimizations	■	■	■
VHDL RTL & VITAL Performance Optimizations	■	■	■
Performance and Memory Profiler	■	■	■
Separate Elaboration	■	■	■
Waveform Management Tool Set	■	■	■
VCD and Extended VCD Support	■	■	■
VCD Re-Simulation	■	■	■
Batch Mode Simulation	■	■	■
Integrated Sim Farm Support (via JobSpy)	■	■	■
Interactive Simulation	■	■	■
Checkpoint & Restore	■	■	■
SWIFT Interface / SmartModels	■	■	■
Synopsys Hardware Modeler Support	■	■	■
Platform Support			
32-Bit OS Support	Linux, Solaris, Windows XP/Vista	Linux, Solaris, Windows XP/Vista	Linux, Solaris, Windows XP/Vista
64-Bit OS Support	Linux x86-64, Solaris 64	Linux x86-64, Solaris 64	Linux x86-64, Solaris 64

1 - Included in SystemC Oaptor

2 - Included with Multi-View Verification Components (MVC)