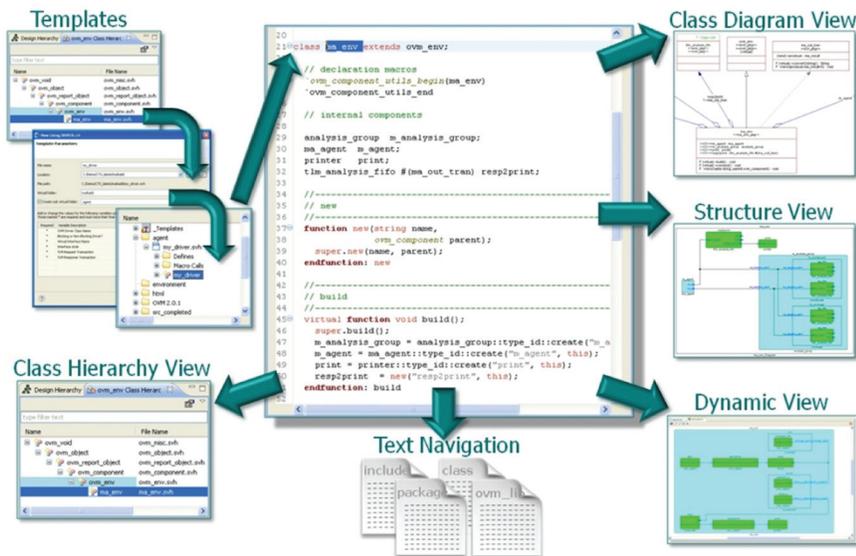


UVM/OVM Testbench Creation and Analysis

Certe Testbench Studio

Testbench Creation

D A T A S H E E T



Certe Testbench Studio delivers a powerful Eclipse-based environment that enables rapid creation and complete understanding of UVM- and OVM-based testbenches.

Create Advanced Verification Testbenches

With complex design work comes the need for advanced testbenches and the necessity for Open Verification Methodology (OVM) and its more recent derivative, Universal Verification Methodology (UVM). Certe Testbench Studio™ is an innovative Eclipse-based integrated design environment that makes it easier to create and comprehend sophisticated SystemVerilog testbenches, enabling designers to leverage all the advantages of UVM/OVM and gain a giant leap in productivity.

UVM and OVM are truly open, interoperable, and proven verification methodologies based on the SystemVerilog IEEE 1800 language. Certe enables hardware and verification engineers to harness the power of UVM/OVM/SystemVerilog by guiding the development of testbenches and registers that are correct-by-construction. Certe augments creation with analysis through deep insight into testbench construction and functionality via connectivity diagrams, multiple class relationship views, and full testbench object browsers.

Certe is a flexible tool designed to handle these complex methodologies in order to establish advanced methodology environments and deliver high quality testbenches in less time. As the design develops, so too does the testbench. Given Certe's creation and construction advantages, detailed analysis features, and build-management capabilities, Certe becomes even more valuable as the testbenches become more complex and advanced. Now designers can easily understand, create, and reuse class- and module-based testbenches, and focus on verifying the design under test (DUT) rather than debugging the testbench.

Correct-by-Construction Creation and Assembly

Testbench code creation is at the heart of Certe and increases hardware and verification engineers' productivity by permitting only legal construction. The "smart" UVM/OVM/SystemVerilog text editor features, which are overlaid to Emacs and Vi via Eclipse plugins, the Template Code Generators, and the testbench-aware nature of Certe, all provide the ability to create correct-by-construction VIP and UVM/OVM testbenches.

BENEFITS:

- Increase productivity in the creation and analysis of extensible testbenches and project register specifications
- Design correct-by-construction testbenches and registers
- Deploy UVM/OVM in a consistent, repeatable manner
- Easily develop and reuse VIP
- Generate consistency in testbench coding
- Reduce testbench development and debug time
- Analyze complex testbenches to improve comprehension
- Automate builds
- Generate documentation
- Eclipse-based application enabling extensibility to third party plugins

PRODUCT FEATURES:

- Eclipse-based for extensibility
- Flexible and scalable Template Code Generators
- "Smart" UVM/OVM code editor
- Visualization of static code and simulated testbench structure
- Analysis of class composition, inheritance and relationships
- UVM, OVM and verification compliance rule checks
- Automatic generation of customized makefile

Template code generation saves time, prevents mistakes and enforces best practices and consistent coding. The Template Code Generators can be customized and are scalable to meet the needs of company guidelines at the corporate, project, and individual user levels. A complete set of templates are supplied in Certe, enabling immediate productivity.

The smart text editor continues the correct-by-construction approach by permitting only legal connections and coding. Auto-complete speeds the entry of unique code, while auto-connect quickly and accurately connects the UVM/OVM elements. Drag-and-drop, class extensions, SystemVerilog interface generation and many other editing features complete the specification of the testbench. Configuring and reconfiguring the testbench using tests, sequences and coverage enables rapid deployment.

Deep Analysis and Understanding

Certe offers many valuable browsers for navigating throughout the testbench. These allow the designer to explore new and reused code through different views of the testbench code with automatic highlighting of the same object within all views.

To identify UVM/OVM and verification coding violations prior to simulation, Certe is preconfigured with a ruleset for testbench design rule checks, ensuring true UVM/OVM compliance during simulation execution.

Visualize Code and Simulated Testbench Structure

The object oriented programming nature of SystemVerilog complicates the testbench construction and analysis. Visualizing the testbench can simplify matters by making it easier to assess testbench composition and functionality. Certe provides views of the code and simulated testbench structure to increase testbench understanding and aid in documentation of any view or browser. Views include:

- UVM/OVM component connectivity
- Simulation UVM/OVM structures
- Class diagram view

Integral to Mentor Graphics Advanced Verification Methodology

Certe complements the Mentor Graphics verification solutions including ReqTracer™, Vista™, Questa® verification platform and HDL Designer™.

Register Definition and Management

The Register Assistant technology delivers register specification and management, extending the Certe correct-by-construction functionality by automatically generating registers and memories in the various formats required by the project. Register Assistant technology also helps to automate the production of register documentation, a critical part of today's designs.

Additionally, the technology manages all register information in a single, cohesive datamodel, accepting inputs from various sources and generating UVM and OVM register package SystemVerilog files. Register Assistant also generates synthesizable RTL and documentation while other generated formats are in development. The correct-by-construction generation eliminates the manual, laborious and error prone hand-edited approach, significantly improving productivity and quality.



Register management and automated generation of the registers and memory in the UVM and OVM Register Package format reduces effort and improves quality.

Platform Support and Availability

Certe is available as a standalone product or combined with the Register Assistant technology for a complete UVM/OVM testbench creation solution. Certe is available for Windows and Linux platforms.

For the latest product information, call us or visit: www.mentor.com/certe

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