

| ModelSim 6.4 Series Product Comparison | | | | |
|---|-----------------------------------|---|---|---|
| Feature | ModelSim Designer | ModelSim PE | ModelSim LE | ModelSim SE |
| | <i>Integrated FPGA Design</i> | <i>Block/Small System Simulation, Windows</i> | <i>Block/Small System Simulation, Verilog & Linux</i> | <i>Large Block/System Simulation, All Platforms</i> |
| General | | | | |
| Licensing - Floating License | Option | Option | Option | ■ |
| Language Neutral License | | | | Option |
| ASIC Sign-Off | | | | ■ |
| Integrated FPGA Library Support | ■ | | | |
| Integrated Version Control | ■ | | | |
| HDL Editor | ■ | ■ | ■ | ■ |
| Integrated Project Manager | ■ | ■ | ■ | ■ |
| Source Code Templates and Wizards | ■ | ■ | ■ | ■ |
| Platform-Independent Compiled Database | ■ | ■ | ■ | ■ |
| Native-Compiled Architecture | ■ | ■ | ■ | ■ |
| Incremental Compilation | ■ | ■ | ■ | ■ |
| 32/64-Bit Cross-Compatibility | | | | ■ |
| Languages | | | | |
| VHDL | ■ | ■ | | ■ |
| Verilog | ■ | ■ | ■ | ■ |
| Mixed Language | Option | Option | | Option |
| Verilog 2001, 2005 | ■ | ■ | ■ | ■ |
| SystemVerilog Design | ■ | ■ | ■ | ■ |
| SystemC 2.2 | | Option | Option | Option |
| Analog/Mixed Signal (Advance MS Product) | | | | Option |
| Verilog PLI/VPI | ■ | ■ | ■ | ■ |
| SystemVerilog Direct Programming Interface | ■ | ■ | ■ | ■ |
| VHDL FLI | | | | ■ |
| Creation | | | | |
| Design Entry | ■ | | | |
| HDL Text to Graphics | ■ | | | |
| Block and State Diagram Editing | ■ | | | |
| Waveform Editor | ■ | | | ■ |
| Stimulus Generation | ■ | ■ | ■ | ■ |
| Debug | | | | |
| Interactive Debug | ■ | ■ | ■ | ■ |
| Post-Simulation Debug | Option | Option | ■ | ■ |
| Enhanced Dataflow Window | Option | Option | ■ | ■ |
| Source Annotation | Option ¹ | Option ¹ | ■ | ■ |
| FSM Debug | ■ | ■ | ■ | ■ |
| C Debugger | | Option ² | ■ | ■ |
| Memory Window | ■ | ■ | ■ | ■ |
| Extra Standalone Viewer | | Option | Option | Option |
| Multiple Waveform Windows | | | | ■ |
| Waveform Compare | Option | Option | ■ | ■ |
| Transaction Viewing (SystemC) | | Option ² | Option ² | Option ² |
| JobSpy | | | | ■ |
| SignalSpy | ■ | ■ | ■ | ■ |
| User-Customizable GUI (via Tk) | | | | ■ |
| Animation of Graphics | ■ | | | |
| Signal Probes on Graphics | ■ | | | |
| Cross Referencing between Windows | ■ | ■ | ■ | ■ |
| Coverage | | | | |
| Code Coverage (with Toggle Coverage) | Option | Option | Option | ■ |
| Unified Coverage DataBase (UCDB) | Option | Option | Option | ■ |
| Coverage Viewer | Option | Option | Option | ■ |
| Test Ranking | Option | Option | Option | ■ |
| Simulation | | | | |
| Single-Kernel Simulation Engine | ■ | ■ | ■ | ■ |
| Verilog RTL & Gate Performance Optimizations | | | | ■ |
| VHDL RTL & VITAL Performance Optimizations | | | | ■ |
| Performance and Memory Profiler | Option | Option | Option | ■ |
| Separate Elaboration | | | | ■ |
| Waveform Management Tool Set | ■ | ■ | ■ | ■ |
| VCD and Extended VCD Support | ■ | ■ | ■ | ■ |
| VCD Re-Simulation | ■ | ■ | ■ | ■ |
| Batch Mode Simulation | | ■ | ■ | ■ |
| Integrated Sim Farm Support (via JobSpy) | | | | ■ |
| Interactive Simulation | ■ | ■ | ■ | ■ |
| Checkpoint & Restore | | | | ■ |
| Verilog 2005 Encryption | ■ | ■ | ■ | ■ |
| SWIFT Interface / SmartModels | Option | Option | | ■ |
| Synopsys Hardware Modeler Support | | | | ■ |
| Platform Support | | | | |
| 32-Bit OS Support | Windows XP/Vista | Windows XP/Vista | Linux | Linux, Solaris, Windows XP/Vista |
| 64-Bit OS Support | | | | Linux x86-64, Solaris 64 |

1 - Included in Enhanced Dataflow Option

2 - Included in SystemC Option