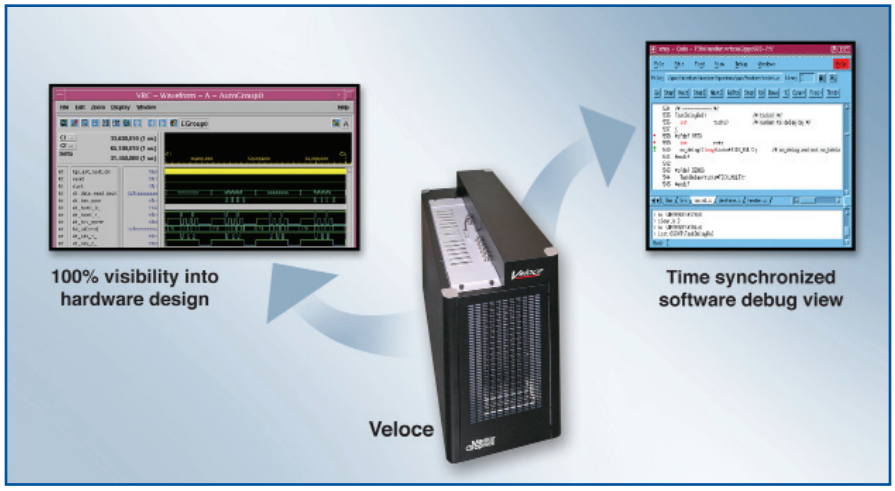
Hardware-Based
Functional Verification

iSolve Solutions for ARM Processors

D A T A S H E E T



Hardware/software co-verification with the Veloce emulator for System-on-Chip designs.

System Verification with Embedded Processors

The Mentor Graphics® iSolve™ Processor solutions for ARM® processors allow a range of Cortex™ embedded and application cores to be used directly in high-performance System-on-Chip (SoC) verification with Mentor Graphics Veloce® hardware emulators.

Processor solutions are available for ARM Cortex-A8, ARM Cortex-A9, and ARM Cortex-A9 dual core. These are supported by using the ARM Logic Tile, which is based on secure FPGA devices.

A significant benefit to this approach (versus connecting a software model of the microprocessor) is that the resulting model is 100 percent complete and accurate. The user of the solution receives a self-contained Target Platform to connect to the Mentor Graphics hardware emulator. In addition, the user also receives a software package containing Verilog netlist files, setup scripts, and design examples — plus full documentation.

PRODUCT FEATURES

- Broad range of ARM embedded and application cores available: ARM Cortex-A8, ARM Cortex-A9, ARM Cortex-A9 dual core
- AMBA standard interface to the design under test in the emulator
- System verification at up to 1 MHz speed (typically)
- Synchronized HW/SW break-points for deterministic debug
- Simple support for designs with multiple ARM processors and with ARM/DSP processor combinations

PRODUCT BENEFITS

- Reduces HW/SW integration and verification effort for designs with embedded processors
- Immediate availability of high performance, high fidelity ARM application and embedded cores
- Replaces custom hardware prototypes with early system level verification stations
- Software integration, verification, and debug at speeds up to 1 MHz
- Connects to industry standard software debug tools, such as ARM DS-5
- Debug designs with multiple processors, including those with DSP devices

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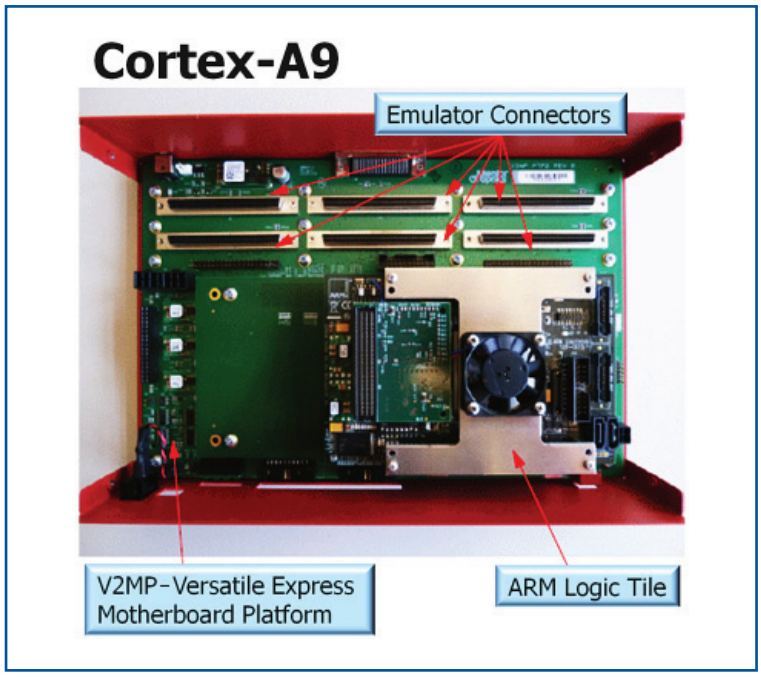
The solution is quick to set up and simple to verify with the examples and test procedures provided. For integration into the design, the user is simply required to include an IP core level Verilog file into the compilation flow.

With the inclusion of one or more ARM microprocessors in the design, verification with Mentor Graphics hardware emulators can be performed at full emulation speed. The user can then connect industry standard, JTAG-based software debug tools to a dedicated connection on the circuit board. This debug connection can also include, for example, connection to DSP devices that are mapped into the logic resources of the emulator.



ARM Cortex-A9 Logic Tile mounted on the iSolve processor solution's motherboard.

Visit our website at www.mentor.com/emulation for more information.

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