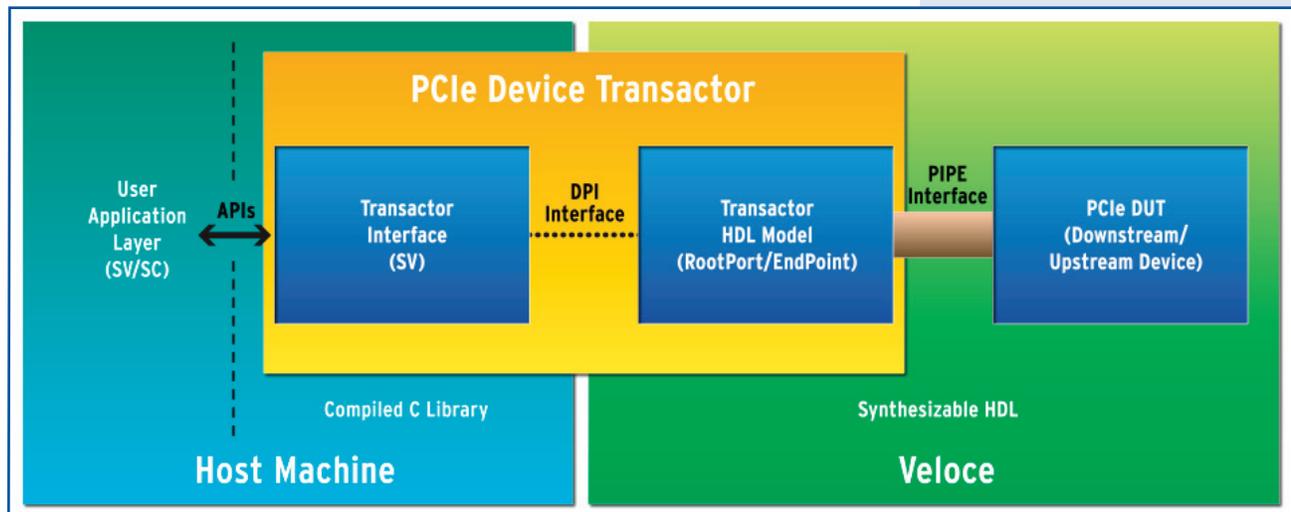


Veloce PCIe Transactor



The Veloce PCIe Transactor provides a SystemVerilog, SystemC, or C interface to interact with the transaction layer of a PCI Express model running in the emulator.

Accelerating Verification of PCIe Protocol Devices

Today's system-on-chip (SoC) designs rely heavily on a variety of industry standard bus protocol interfaces. To help you achieve the required standards of productivity and higher levels of effectiveness in the verification of these standard interfaces within complex SoC designs, Mentor Graphics® offers the Veloce® PCIe Transactor for PCI Express device verification.

The Veloce PCIe Transactor provides a SystemVerilog, SystemC, or C interface to interact with the transaction layer of a PCI Express model running in the Veloce emulator. The transactor can be configured and used as either a PCIe root port or a PCIe endpoint device. Each use mode for the PCIe Transactor generates the appropriate stimulus for the SoC design-under-test (DUT) executing in Veloce: opening connections and creating and exchanging commands and transactions for tests.

Additionally, the Veloce PCIe transactor allows the use of UVM-based verification environments, where sequences exercise the transaction interface.

Designed to connect directly to high-performance emulation environments, Veloce transactors deliver acceleratable verification IP (VIP) that runs up to 10,000 times the speed of pure software simulation, significantly reducing verification times and regression testing for increased productivity.

PRODUCT FEATURES

- Flexible, easy-to-use transactors for use with Veloce emulators and Questa® simulators
- Optimized for high-speed emulation performance
- PCIe root port and endpoint devices supported
- Link widths of x1, x4, and x8 lanes supported
- PCIe base specification 3.0, 2.0, 1.1 revision compliant
- 32-bit PCIe PIPE interface for all link widths is provided
- Debug features (such as, checkpoint save/restore) enable high-levels of productivity
- Usage examples provided to get up and running quickly
- Supports both RTL and TLM abstraction levels

PLATFORMS SUPPORTED

- Veloce family of emulators
- RHEL4, SuSE 10 Linux

This easy and convenient to use transactor helps you reduce overall testbench development time and complete more verification with less effort. You no longer have to spend time on standard protocol functionality, giving you more time to focus on the features that differentiate your designs.

Deliverables

- Encrypted HDL module of the PCIe Transactor for use in Veloce emulation and Questa simulation environments.
- A NULL-PHY module. This can be connected to a PCIe PIPE compliant DUT interface.
- C library of the transactor to be loaded or compiled for Questa and Veloce.
- SystemC and SystemVerilog interfaces for integrating the transactor with an application layer.
- UVM-based transaction layer sequences are provided in the package (compatible with Questa VIP models).
- Examples and documentation showing usage in C, SystemC, and SystemVerilog testbenches.

Visit our website at www.mentor.com/emulation for more information.

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