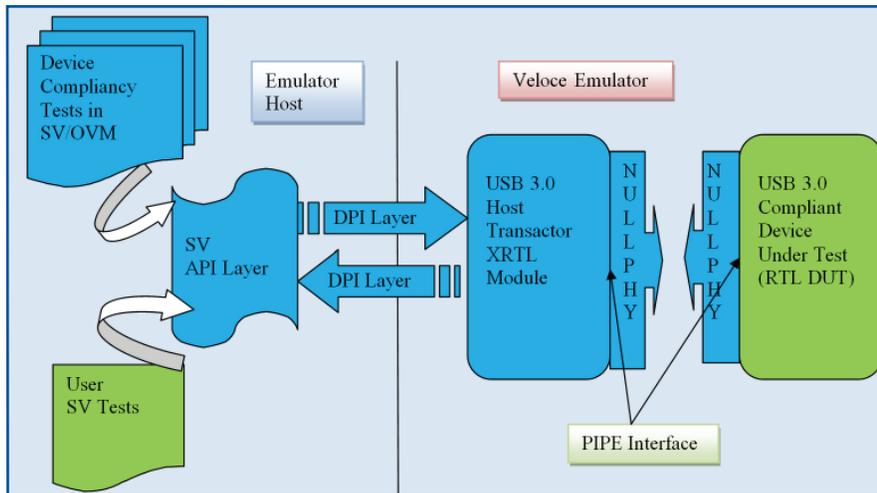


Veloce USB 3.0 Host Transactor



Veloce USB 3.0 Host Transactors can be instantiated in HDL and connected to the SuperSpeed peripheral port of the DUT in the emulator.

Accelerating Verification of USB 3.0 Protocol Devices

Today's system-on-chip (SoC) designs rely heavily on a variety of industry standard bus protocol interfaces. To help you achieve the required standards of productivity and higher levels of effectiveness in the verification of these standard interfaces within complex SoC designs, Mentor Graphics® offers the Veloce® USB 3.0 Host Transactor.

The Veloce USB 3.0 Host Transactor provides the host interface to a USB 3.0 SuperSpeed compliant device under test (DUT) inside a Veloce emulator. It generates the appropriate stimulus for the DUT SoC executing in Veloce, passing packets (or transactions) of protocol data for tests. The transactor also provides fully documented, high-level APIs and example tests to model a test environment that can exercise the emulated USB 3.0 device.

Designed to connect directly to high-performance emulation environments, Veloce transactors deliver speeds in emulation up to 10,000 times that of pure software simulation, significantly reducing verification times and regression testing for increased productivity.

PRODUCT FEATURES

- Flexible, easy-to-use transactor for use with Veloce® emulators and Questa® simulators
- Optimized for high-speed emulation performance
- Stimulus generation
- Protocol checking with provided SystemVerilog/OVM USB compliancy tests
- Supports SystemVerilog HVL testbench environments through a set of initialization and USB transfer APIs
- Usage examples provided to get up and running quickly
- Supports both RTL and TLM abstraction levels

PLATFORMS SUPPORTED

- Veloce family of emulators
- RHEL4, SuSE 10 Linux

The Veloce USB 3.0 Host Transactor provides built in OVM compliancy sequences which can be used to check the emulated USB 3.0 device's compliancy with the protocol standard. The transactor can also be used in a SystemVerilog HVL testbench and provides high level APIs for this purpose; for example, SCSI read/write APIs and other USB initialization/control/data transfer APIs.

The Veloce USB 3.0 Host Transactor delivers a protocol-specific scalable verification solution that can be used for RTL, TLM, and system-level verification.

The Veloce Transactors are easy and convenient to use, helping you reduce overall testbench development time and complete more verification with less effort. You no longer have to spend time on standard protocol functionality, giving you more time to focus on the features that differentiate your designs.

Deliverables

- Encrypted HDL module of the Host Transactor for use in Veloce emulation and Questa simulation environments.
- An open source NULL-PHY module. This can be connected to a PIPE compliant DUT interface.
- C library of the transactor to be loaded or compiled for Questa and Veloce.
- SystemVerilog Interface with integrated components for SV/OVM testbenches and device compliancy tests, with examples and documentation.

Visit our website at www.mentor.com/emulation for more information.

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