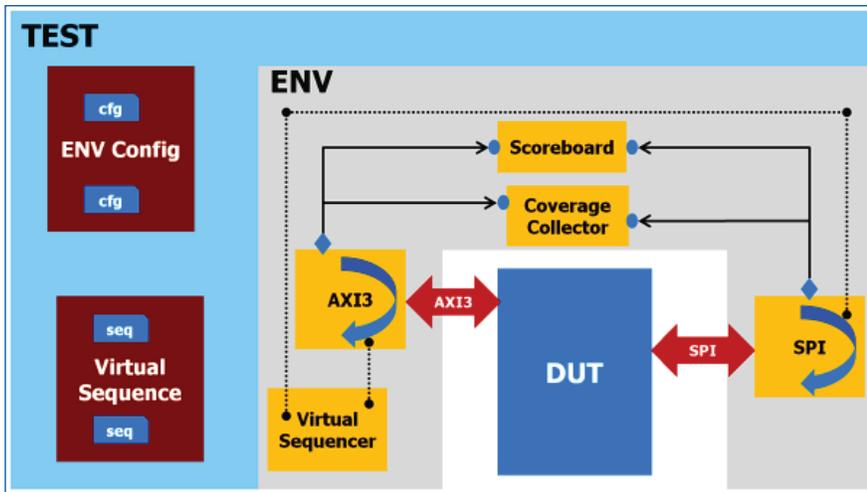


# Veloce Base Transactor Library



One or more of the Veloce standard bus protocol transactor modules can be instantiated in HDL and connected to a DUT.

## Accelerating Verification of Standard Bus Protocol Devices

Today's system-on-chip (SoC) designs rely heavily on a variety of industry standard bus protocol interfaces. To help you achieve the required standards of productivity and higher levels of effectiveness in the verification of these standard interfaces within complex SoC designs, Mentor Graphics® offers the Veloce® Base Transactor Library.

The Veloce Base Transactor Library comprises a catalog of standard bus protocol models for use with a variety of testbenches. These transactor models generate the appropriate stimulus for the SoC executing in Veloce, passing packets (or transactions) of protocol data for tests.

Designed to connect directly to a high-performance emulation environment, Veloce transactors deliver acceleratable verification IP (VIP) that runs up to 10,000 times the speed of pure software simulation, significantly reducing verification times and regression testing for increased productivity.

The Veloce Base Transactor Library models can be used in various HVL testbench environments, including SystemC and SystemVerilog, and deliver the stimulus generators, monitors, and scoreboarding capabilities as used with the popular OVM/UVM standards.

### PRODUCT FEATURES

- Flexible, easy-to-use models for use with Veloce® emulators and Questa® simulators
- Optimized for high-speed emulation performance
- Stimulus generation
- Protocol checking
- Test suite, compliance tests
- OVM coverage collectors and monitors
- Delivers support for various HVL testbench environments, such as SystemC and SystemVerilog, including OVM and UVM
- Usage examples provided to get up and running quickly
- Multiple models (instances) with a single runtime license
- Supports both RTL and TLM abstraction levels

### PROTOCOLS SUPPORTED

- I<sup>2</sup>C
- I<sup>2</sup>S
- SPI
- AMBA 3
- AXI-4

### PLATFORMS SUPPORTED

- Veloce family of emulators
- RHEL4, SuSE 10 Linux

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The Veloce Base Transactor Library delivers a scalable verification solution for popular protocols and standard interfaces that can be used for RTL, TLM, and system-level verification. All models have been stress tested using multiple threads and constrained random stimuli and will achieve 100 percent protocol coverage.

The easy and convenient to use Veloce transactors help you reduce overall testbench development time and complete more verification with less effort. You no longer have to spend time on standard functionality, giving you more time to focus on the features that differentiate your designs.

## Deliverables

- Encrypted HDL modules for use in Veloce emulation and simulation environments, such as Questa®.
- C library to be loaded or compiled for Questa using *tbxsvlink*.
- SystemVerilog interface with integrated components for SV/OVM/UVM testbenches.
- SystemC interface for integrating the transactor in a SystemC environment.
- Examples and documentation showing usage in SystemVerilog/OVM, UVM, and SystemC environments.

Visit our website at [www.mentor.com/emulation](http://www.mentor.com/emulation) for more information.

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