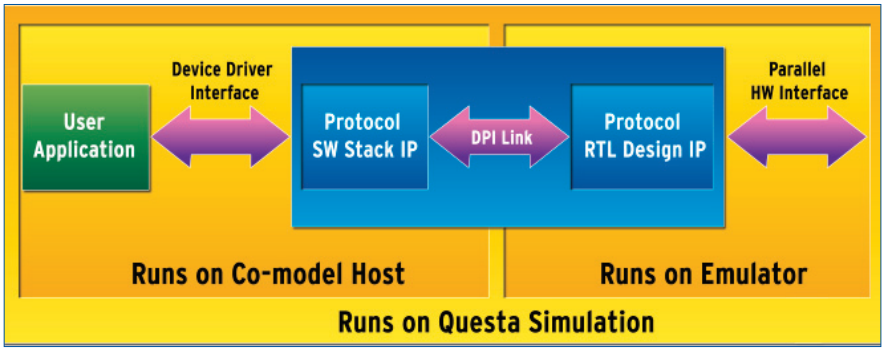
New Generation of Emulation Solutions

Veloce VirtuaLAB

Veloce VirtuaLAB Products

D A T A S H E E T



Veloce VirtuaLAB emulation solutions provide software-based, full applications for the verification of complex SoCs without the need for external hardware.

Solving the Verification Needs of SoC Designers

Veloce® VirtuaLAB is a new concept for emulation verification, delivering multiple application solutions that provide a "virtual lab" environment to verify complex, System-on-Chip (SoC) designs having multiple chip interfaces. These include networking, multimedia, USB, and other bus-protocol applications commonly found in products such as tablet PCs, netbooks, digital set top boxes, game consoles, smartphones, network switches/routers, and others. VirtuaLAB delivers a family of such applications to the SoC verification engineer, creating a non-intrusive and high-performance lab environment that is reproducible, expandable, and readily available for sharing between multiple verification teams.

VirtuaLAB eliminates the need to connect external hardware peripherals to a Veloce emulator, as is necessary with traditional In-Circuit Emulation (ICE). Instead, part of the peripheral is modeled in the emulator and part of it is modeled as an application in a workstation. Through Mentor's industry-leading co-modeling technology, a connection from a "virtual device," such as an Ethernet model, is made to the user's design-under-test (DUT) executing in Veloce. High-throughput, multiple co-model channels enable high-speed emulation of the customer design, using, for example, virtual Ethernet traffic as a stimulus under direct user control. This significantly reduces verification times over software simulation methods.

FEATURES AND BENEFITS:

- High-performance verification using Veloce family of emulators
- Virtual traffic generators execute specific test scenarios to stress-test SoC designs
- VirtuaLAB applications shared across multiple teams worldwide
- Solution-specific hardware and test equipment connected to the Veloce emulator eliminated
- No cabling constraints, no cables
- Richly-featured analysis tools ease debug of designs
- Easy-to-use GUI boost verification productivity
- Batch mode option enables regression testing and delivers high verification productivity
- Latest-generation protocol standards supported
- Verify multiple protocols in an SoC design
- Multiple virtual application solutions, including:
  - Multimedia video/audio standards
  - Multi-Gigabit Ethernet
  - USB
  - PCI Express

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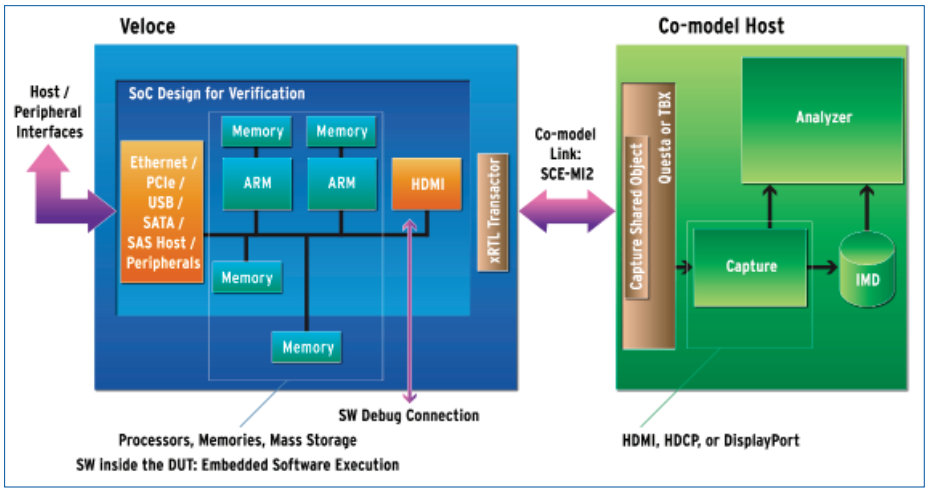
VirtuaLAB Applications Provide Test, Visibility, and Control Capabilities

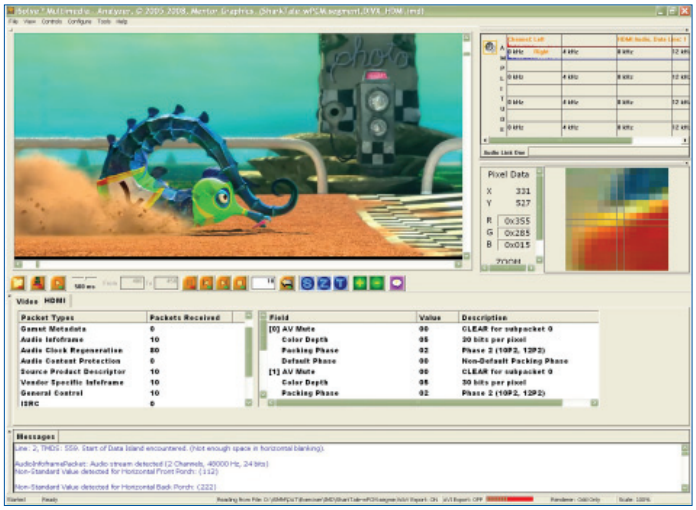
The flexible approach to verification testing adopted by VirtuaLAB allows customers to choose a variety of options for generating stimulus and verifying designs. These allow development of very specific stimuli that "stress test" a design by creating a stream of customized packets of specific data derived from industry-standard files. For example, a multimedia device DUT could be exercised by HDMI packets derived from .avi files.

Analysis tools capture and graphically analyze the video and audio output of the design running in Veloce and extract important data for debugging the SoC. This entire "virtual" flow delivers a significant improvement in productivity over existing emulation verification methods.

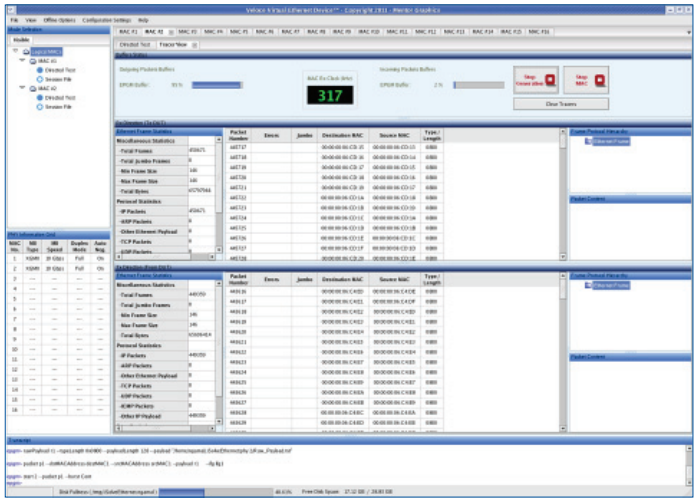
Configuration and execution of packet or data streaming is performed either from a GUI or from TCL-commands; the latter is especially useful for regression testing.



A typical environment for the analysis of SoC designs using a VirtuaLAB application, in this case, for a multimedia DUT.



VirtuaLAB GUI for video and audio analysis.



VirtuaLAB GUI for Ethernet device analysis.

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