

# iSolve ARM Processor Solutions

## Hardware-Based Functional Verification

D A T A S H E E T



100% visibility into  
hardware design

Veloce

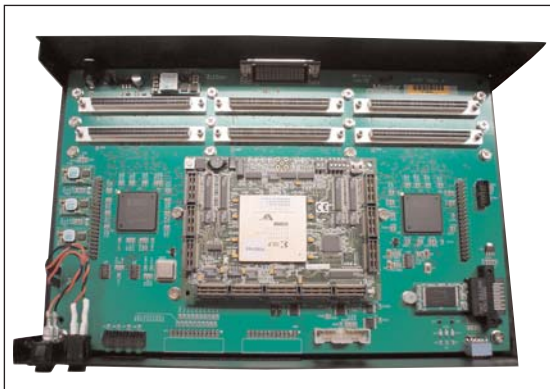
Time synchronized  
software debug view

Hardware/software co-verification with the Veloce emulator for System-on-Chip designs.

### System Verification with Embedded Processors

The Mentor Graphics® iSolve™ ARM Processor solutions allow a broad range of ARM7, ARM9, ARM11, and Cortex embedded and application cores to be used directly in high-performance System-on-Chip (SoC) verification with Mentor Graphics hardware emulators.

A range of hard macro microprocessors are available including the ARM7TDMI and ARM11MPCore. These microprocessors are based on bonded-out cores that are mounted on to a circuit board and then connected through the emulator



An ARM926EJ-S Logic Tile mounted onto the ARM processor solution's motherboard.

input/outputs. Also available are ARM9x6E (J)-S and ARM1176JZ(F)-S cores supported by using the ARM Logic Tile, which is based on secure FPGA devices. A significant benefit to this approach (versus connecting a software model of the microprocessor) is that the

### Major product features:

- Broad range of ARM embedded and application cores available: ARM7TDMI, ARM926EJ-S, ARM946E-S, ARM1176JZF-S, ARM11MPCore, Cortex R4, A8
- AMBA AHB standard interface to the design under test in the emulator
- System verification at 500kHz - 1 MHz speed (typically)
- Synchronized HW/SW breakpoints for deterministic debug
- Capability to plug up to three ARM9x6E(J)-S microprocessors into a single IP-Xpress board
- Simple support for designs with multiple ARM processors and with ARM/DSP processor combinations

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Graphics®**

resulting model is 100% complete and accurate. The user of the solution receives a self-contained Target Platform to connect to the Mentor Graphics hardware emulator. In addition, the user also receives a software package containing Verilog netlist files, setup scripts, and design examples – plus full documentation.

The solution is quick to set up and simple to verify with the examples and test procedures provided. For integration into the design, the user is simply required to include an IP core level Verilog file into the compilation flow.

With the inclusion of one or more ARM microprocessors in the design, verification with Mentor Graphics hardware emulators can be performed at full emulation speed. The user can then connect industry standard, JTAG-based software debug tools to a dedicated connection on the circuit board. This debug connection can also include, for example, connection to DSP devices which are mapped into the logic resources of the emulator.

### Product benefits:

- Reduces HW/SW integration and verification effort for designs with embedded processors
- Immediate availability of high performance, high fidelity ARM application and embedded cores
- Replaces custom hardware prototypes with early system level verification stations
- Software integration, verification, and debug at speeds up to 1MHz
- Connects to industry standard software debug tools such as ARM RealView
- Debug designs with multiple processors including those with DSP devices

Visit our web site at [www.mentor.com/emulation](http://www.mentor.com/emulation) for more information

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