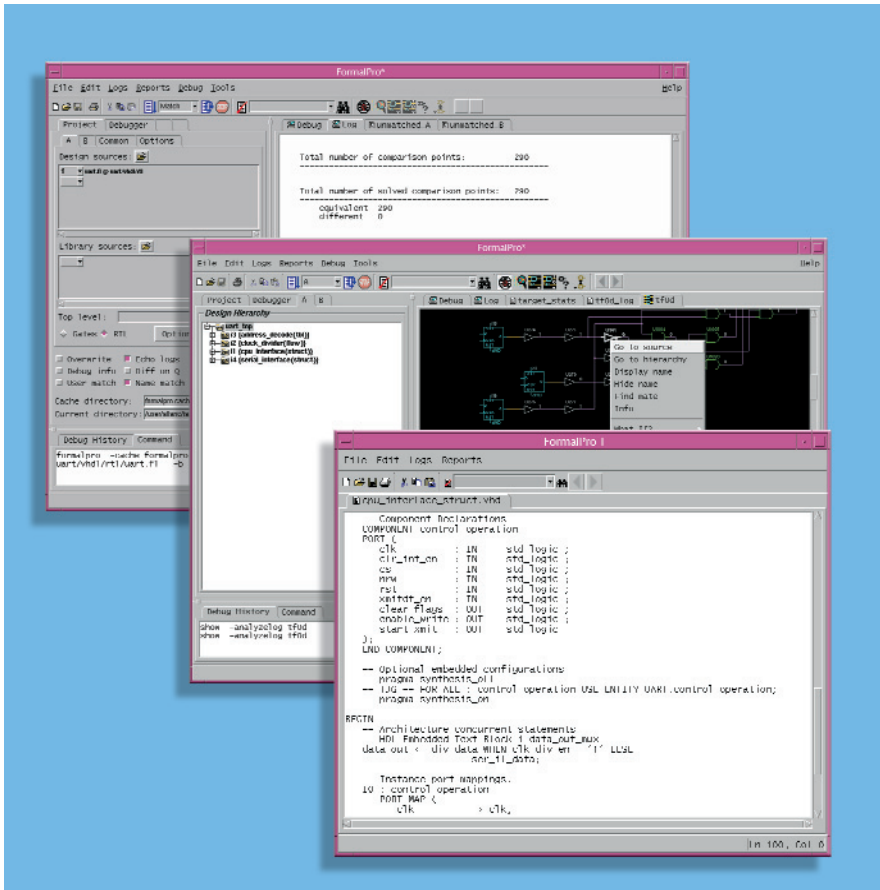


# FormalPro

## D A T A S H E E T



The FormalPro equivalence checker saves weeks in the verification of ASICs and ICs.

## Complete Solution for Gate-Level Regression Testing of ASICs and ICs Larger than 100,000 Gates

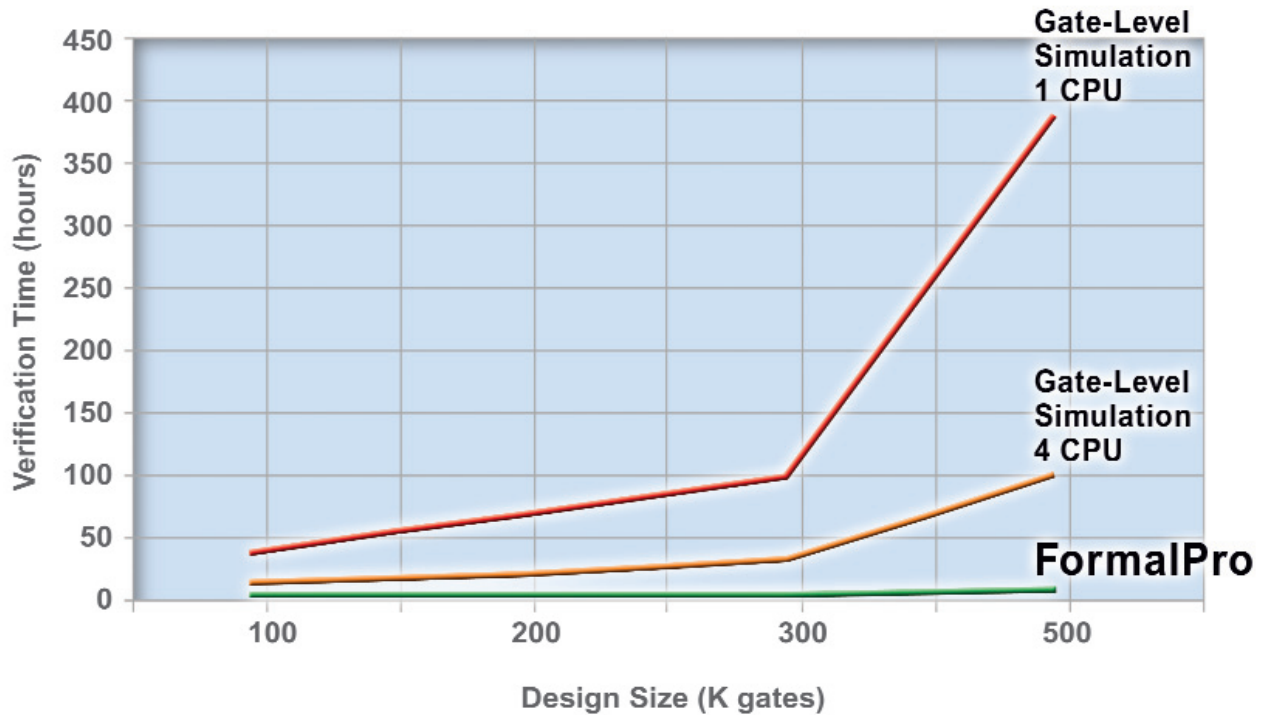
FormalPro™ is the Mentor Graphics solution for gate-level regression testing of ASICs and ICs of 100,000 gates or more. FormalPro uses static formal verification techniques to prove that a design is functionally identical to its golden reference. This technique is orders of magnitude faster than traditional gate-level simulation. Designs that take days or even weeks to simulate with gate-level simulation can be verified in hours or even minutes using FormalPro. For designs greater than 100,000 gates, FormalPro is an essential verification tool in an ASIC design flow.

### Gate-Level Regression Testing

Regression testing is the process of verifying that a design behaves as desired, and as previously validated, while it undergoes modification in the implementation phase. When in the RTL domain, this means re-simulating the design with hundreds or even thousands of pre-written tests to ensure that it still passes every

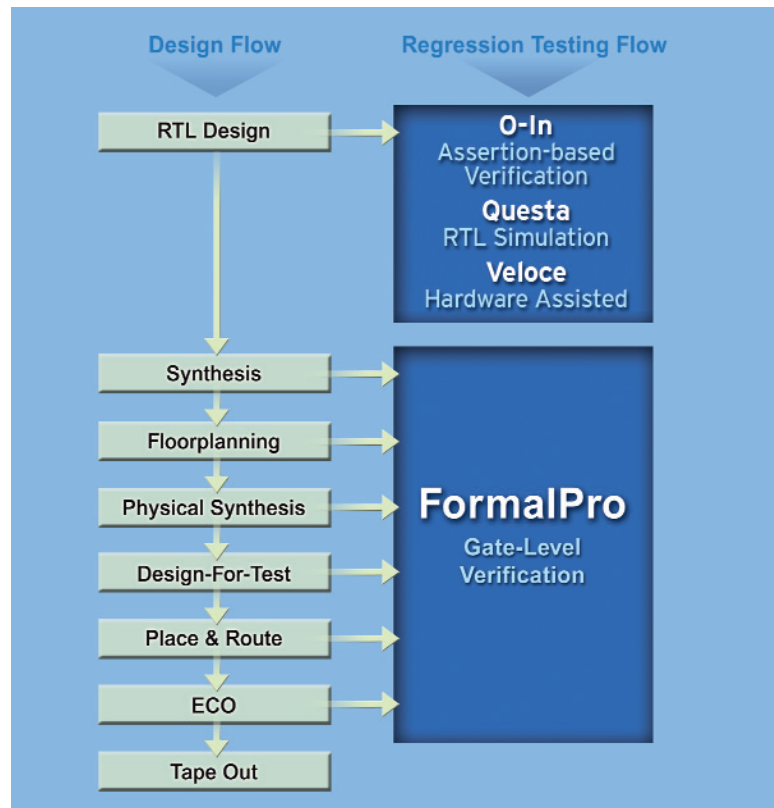
### Major product features

- 100 percent verification coverage without testbenches
- Full-chip verification of all designs from FPGAs to multimillion-gate SoCs
- FPGA support for Altera, Actel and Xilinx products with automatic setup flows
- Power Aware verification confirms that PCF and UPF constraints are followed
- Ultra high capacity ensures verification of physical superchip flows without manual partitioning
- Distributed multiprocessor capability accelerates verification of the largest multimillion-gate designs
- Comprehensive debug tool identifies the exact location and cause of design errors
- Unique “what-if” capability investigates design modifications within the existing verification session
- Verification restart feature further reduces verification time by eliminating the need to recompile and rerun the entire verification with each incremental design and set-up changes
- Intuitive graphical user interface guides user through all stages of verification set up



FormalPro performs gate-level regression testing orders of magnitude faster than gate-level simulation.

time a modification is made. These simulations take many hours per test; however, this can be alleviated by running multiple simulations in parallel. When the design goes to the implementation process — through logic synthesis and back-end physical implementation — regression testing at the gate-level requires a different methodology. The increase in volume of data from a few thousand lines of RTL code to hundreds of thousands of interconnected cells means that simulations can take days, weeks, or even months. FormalPro is a regression testing tool that verifies that a design, after undergoing each of the implementation steps, is functionally identical to a previously signed off reference model. This methodology is orders of magnitude faster than simulation, ensuring that regression testing of designs at the gate-level can be performed in comparable if not faster runtimes than RTL regression tests.



FormalPro works in conjunction with 0-In®, Questa® and Veloce® to form a scalable digital regression testing flow.

## 100% Verification Coverage

FormalPro uses static verification algorithms to guarantee verification of 100 percent of the design, independent of testbenches. Unlike simulation, which tests nothing unless directed to by a testbench, FormalPro verifies every node in the design against the reference model (unless specifically directed not to). This ensures that even the subtlest introduced errors — for example, connectivity changes in the place-and-route process that alter functional behavior — are identified and reported.

## Full-Chip Verification

FormalPro's algorithms enable full-chip designs to be verified in their entirety. As designs pass through the physical implementation process, tools often optimize the design's hierarchy to meet timing-performance requirements. Therefore, an exact correspondence between lower-level blocks in a design is not possible. FormalPro's full chip methodology ensures that all designs, from 100,000 gates to beyond 50 million gates, can be verified in one process, without having to manually partition the design. 32-bit and 64-bit operating modes are provided.

## FPGA Verification

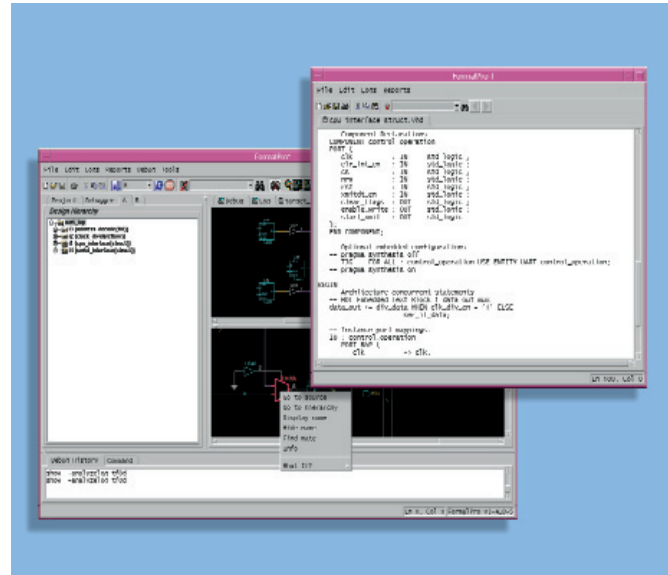
FormalPro has built-in support and licensing options for FPGA equivalence checking. These FPGA vendors provide verification-compatible library files: Xilinx, Actel, Altera. FPGA synthesis tools can provide a verification guide file to automate the setup of a FPGA project and provide constraints for encodings, register duplication, name mapping and more. FormalPro has support for the Mentor Graphics FVI format, and VIF and VSDC formats from Synopsys. Customer Support can assist with conversion of additional guide formats.

## Power Aware Verification

Accellera's UPF and Mentor Graphics PCF power aware specification formats are supported for RTL-to-gate and gate-to-gate comparisons of power specification to power implementation. Example checks include power domain register type checks and preservation of isolation buffers for power domain crossings.

## Debug Tool — The Shortest Route to a Correct Design

FormalPro's debugging capabilities dramatically reduce overall verification time by enabling engineers to identify and correct a faulty design hours or even days faster than other tools.



*FormalPro's debug capabilities include cross-probing between schematics and RTL source code to trace design errors.*

## Debug Features

- Identifies exact location of error
- Hierarchy browser
- Schematic display
- Cross probing reports to gates to RTL to schematics
- Provides difference vector for use in a simulator
- FormalEyes Hazard checks report

## Unique What-If Capability Tests Design Modifications in Minutes

Once the cause of an error has been identified, FormalPro's unique what-if capability enables engineers to investigate design modifications within the existing verification session. When a functional difference has been reported, the user tests assumptions on how to resolve the problem using the what-if function. This capability saves hours, even days, in both debug time and the duration of iterations.

## Verification Restart

FormalPro provides a full verification restart capability. By allowing engineers to restart the tool at any stage in the verification process, FormalPro further reduces verification time by ensuring that only the processing directly related to a design or set up change is rerun.

## Standard Language Support

FormalPro supports standard languages including VHDL-93 and 87, Verilog-2001, Verilog-95, SystemVerilog, Liberty, Mentor-atpg.

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## Platform Support

FormalPro is supported on Sun Solaris™  
and Linux® based workstations.

**Visit our web site at [www.mentor.com/formalpro](http://www.mentor.com/formalpro) for more information, articles, or white papers.**

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