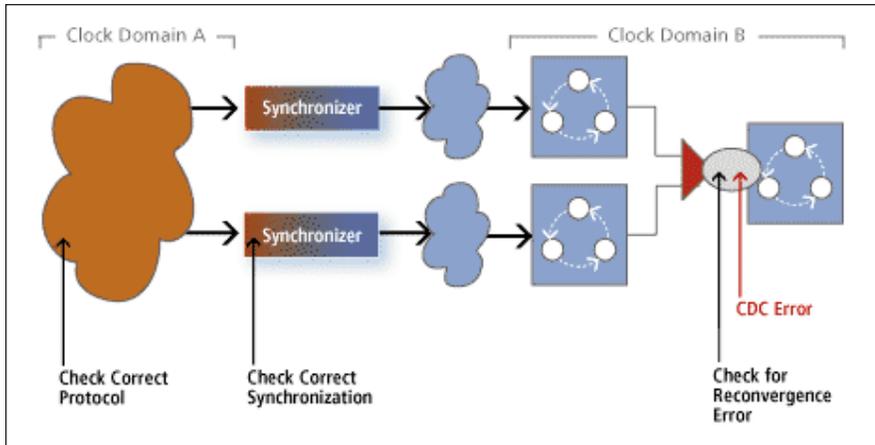


# 0-In Clock-Domain Crossing



0-In CDC is the industry's most comprehensive and easy-to-use clock-domain crossing verification solution, integrating advanced verification engines with a proven methodology.

## The CDC Verification Challenge

Modern system-on-chip (SoC) designs typically contain many separate clock domains. In hardware, clock-domain crossing (CDC) signals are often subject to the effects of metastability. However, the effects of metastability cannot be analyzed using conventional RTL simulation. As a result, many CDC-related functional bugs go undetected until post-silicon verification.

Designs with CDC signals encounter three fundamental types of problems — all are caused by metastability. The first problem is *propagation of metastability*. To avoid this, designers use synchronizers to reduce the probability that metastability leaks into general logic throughout the design. The second problem is *corruption of data* transferred across clock domains. To avoid this, designers implement CDC protocols designed to ensure proper transmission and reception of data. The third problem is *incorrect logic function where CDC signals reconverge* (i.e., CDC combinational and sequential reconvergence). To avoid this, designers must ensure that their designs are tolerant of the variable delays that occur on each of the reconvergent paths. Using 0-In<sup>®</sup> CDC, designers can verify that their designs are free of all three types of CDC problems.

## Ease of Use

0-In CDC accepts a wide variety of coding styles, including non-synthesizable constructs common in early stages of designs. In addition, 0-In CDC can be run early in the design process, in a fully static mode, with no testbench.

0-In CDC supports simulator command line arguments, so integration into existing design environments is simple. 0-In CDC is fast and has large capacity, so it can be used after every design change, before code check-in. 0-In CDC makes an ideal regression tool.

## Major product features:

- Automated solution for complete CDC verification
- Identifies all clock domains, including derived clocks and gated clocks
- Supports flattened and hierarchical approach to maximize turn-around time and productivity
- Identifies all CDC synchronizers, including structured, ad-hoc, FIFO, handshake, and user-defined synchronizers
- Highlights missing and incorrect CDC synchronization
- Detects and reports combinational and sequential reconvergent CDC signals
- Automatically generates CDC protocol monitors with built-in coverage support
- Automatically proves CDC protocols or allows you to verify protocols in simulation
- Exhaustively verifies CDC functionality using formal verification technology
- Unique CDC-FX technology automatically detects functional errors due to reconvergence
- Includes the most advanced and easiest to use GUI in the industry to analyze and debug CDC problems

## CDC Static Analysis

0-In CDC uses fast static RTL analysis to automatically identify and report all clocks (including gated and derived clocks), all clock domains, all signals crossing clock domains, and all synchronizers (including user-defined synchronizers). 0-In CDC also reports all missing and ad-hoc synchronizers.

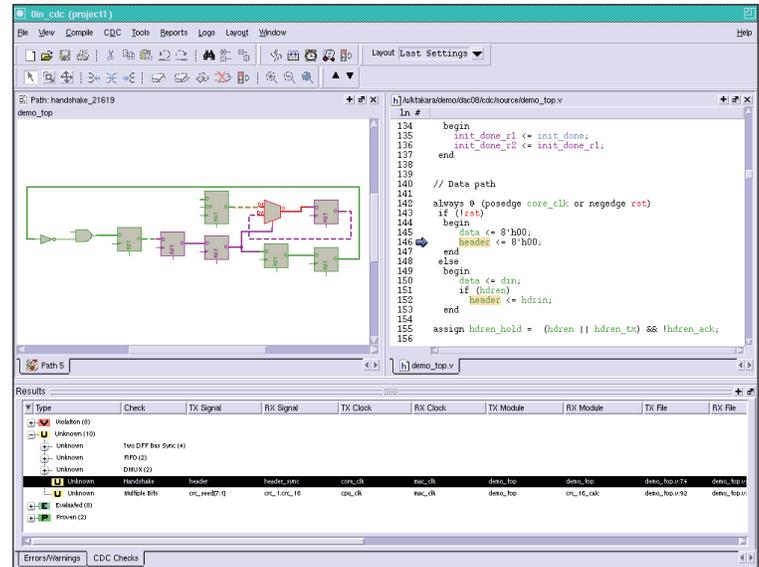
Furthermore, 0-In CDC is unique in that it can analyze designs hierarchically. This has two major benefits. It dramatically improves verification productivity by re-analyzing only those portions of a design that have actually changed, and it removes any potential limit on processing capacity—even the biggest designs are no problem for 0-In CDC.

## CDC Protocols

While proper synchronizer placement ensures that metastability does not leak into general logic, it does not by itself ensure correct CDC functionality. Every signal that crosses clock domains must adhere to an appropriate CDC protocol. Otherwise, transferred data will be corrupted in the presence of metastability in the hardware. For example: A single-bit control signal transmitted out of a fast clock domain must stay stable long enough to be sampled by a slower receiving clock domain (i.e., the control signal must be stable longer than one receiving clock period).

0-In CDC automatically generates protocol monitors for popular CDC design styles, including: single-bit control signals crossing domains via 2DFF synchronizers, multi-bit data signals crossing domains using 2DFF synchronizers, mux-synchronized data/control signals, handshake synchronizers, and FIFO synchronizers.

The automatically generated CDC protocol monitors are either proven by 0-In CDC or verified in the existing simulation environment. In simulation, these monitors detect all violations that might lead to corruption of transferred data. Additionally, these monitors gather coverage information that helps assess how thoroughly the design has been tested for correct CDC functionality.



*0-In CDC provides the industry's most comprehensive analysis and debug.*

## CDC Reconvergence

Metastability causes the transitions of received CDC signals to experience variable and unpredictable delays that do not exist in standard RTL simulations (they only manifest themselves in hardware). These variable delays can cause the logic that recombines the CDC signals — either combinationally or after sequential delays — to fail. As a result, when the design is implemented in silicon it may experience functional problems.

0-In CDC combines powerful static reconvergence analysis with a unique CDC-FX capability. CDC-FX allows existing RTL simulations to be used to verify a design's tolerance to metastability effects on reconvergent paths, automatically identifying problems that would otherwise go undetected until hardware is available. CDC-FX includes comprehensive coverage metrics to gauge the effectiveness of the test suite being used.

## Advanced Debugging Options

0-In CDC provides advanced, interactive analysis and graphical debugging tools as well as concise textual reports, using familiar schematics, source code annotation, and/or waveforms where appropriate.

**Visit our web site at [www.mentor.com/products/fv/abv/0-in](http://www.mentor.com/products/fv/abv/0-in) for more information.**

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