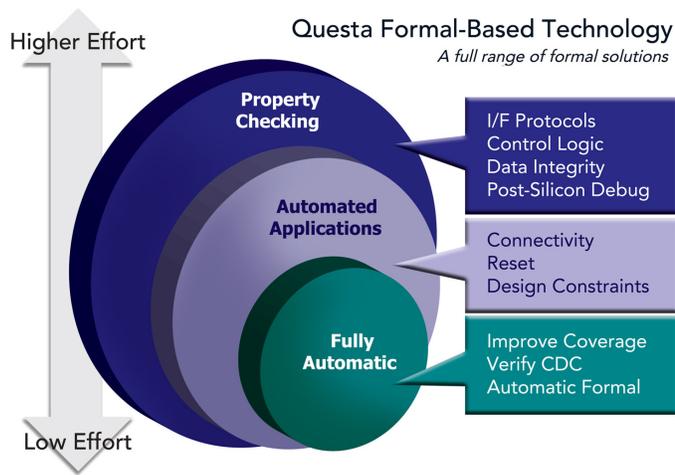


# Questa Formal-based Technologies



Questa offers a broad spectrum of formal solutions, ranging from fully automatic applications such as clock-domain crossing verification, code coverage closure and automatic formal checking to high-powered, highly customizable property checking. These solutions work well by themselves or as a complement to dynamic simulation.

## Broad adoption of formal technology

A handful of IC designers began performing formal verification, proving the correctness of a design's underlying algorithms via mathematical proofs, back in the early 1990s. At that time, formal verification was more or less a completely manual process of writing assertions to do property checking. A decade later, formal applications began to appear that at least partially automated the task of generating assertions. Now, considering the full suite of capabilities in Questa Formal-based technologies, fully automatic push-button formal verification has finally and unequivocally arrived. This means that today the benefits of formal verification, particularly as a complement to dynamic simulation, are available to a wider base of users than ever before.

## Three categories of verification technologies and tools

The Questa Formal-based Technology suite offers users a choice of formal verification technologies and tools ranging from push-button applications to more advanced property checking. The three categories are:

**Fully automatic.** All properties and design intent are inferred by the software. There are three fully automatic tools in the Questa Formal suite: Questa CoverCheck, addressing issues of code coverage closure; Questa Clock-Domain Crossing Verification; and Questa AutoCheck, which performs formal analysis directly on the RTL.

**Automated applications.** Assertions are synthesized from a combination of automatic RTL design analysis and a high level specification of design intent. The properties are then exhaustively verified with formal analysis. The Questa Formal suite includes applications to address issues such as connectivity, X-states, reset structures and design constraints.

**Property checking.** Users write properties and constraints and then run the Questa Formal suite's property checking engines, among the industry's most powerful. This allows for advanced methods, such as abstraction, decomposition, assume-guarantee and waypoints. Manual property checking can also address issues of I/F protocols, functional coverage, control logic, data integrity and post-silicon debug, which in sum provide the most exhaustive possible analysis of a design.

## FEATURES AND BENEFITS:

### Fully automatic applications

- Code coverage closure (Questa CoverCheck)
- Clock-domain crossing (Questa CDC)
- Automatic formal (Questa AutoCheck)

### Accelerated bug discovery

- No need to wait for simulation bringup
- Direct identification of root cause

### Accelerated coverage of design states

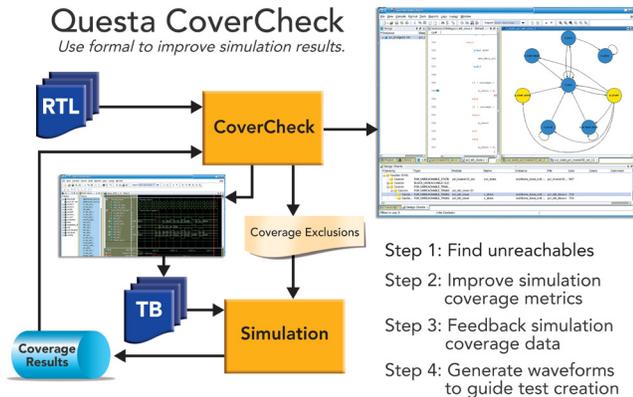
- Not limited by time required to simulate all combinations
- Not limited by assumptions of what to test for

### Complements dynamic simulation

- Metastability
- X-states

## Introducing Questa CoverCheck

Questa CoverCheck dramatically improves the process of achieving code coverage closure. Even after running a comprehensive set of tests in simulation, there typically remains some small fraction of uncovered code. CoverCheck addresses this problem, helping determine whether to skip this code or to enhance the test environment until it is hit.



*Questa CoverCheck methodology. The tool applies formal methods to target code that's unreachable by the simulator.*

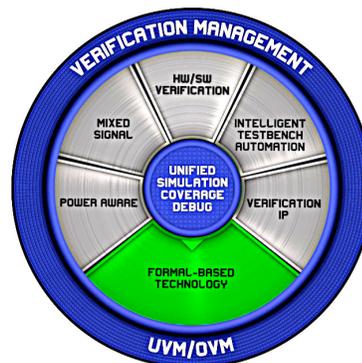
CoverCheck reads the code coverage results stored in the Unified Coverage Database (UCDB) after a simulation run. Then it uses formal methods to specifically target the unreachable code. One possibility: CoverCheck can prove that the targeted code will, in fact, never be exercised. Another: if the code can be reached by formal methods, CoverCheck, by showing the waveform of the stimulus, provides the necessary guidance for a designer to enhance his testbench and check that portion of the design on the next run of the simulator. And since CoverCheck flags code coverage items that are difficult to reach by formal techniques and haven't been hit in simulation, it thus provides a valuable measure of verification complexity. CoverCheck works as a standalone formal verification product and is integrated with the dynamic simulation capabilities in the Questa Advanced Verification Platform.

## Questa Clock Domain Crossing (CDC) Verification

Questa CDC offers comprehensive analysis that eliminates errors in terms of synchronization, CDC protocol and CDC reconvergence. It offers the industry's most advanced CDC analysis with superior performance, capacity and ease of use. Questa CDC includes a CDC-centric advanced debugger for graphical analysis and it recognizes all the commonly used synchronization schemes. It also accepts Synopsys Design Constraints (SDC) files to define clocks, I/O port domains and modes of operation. A TCL shell and set of directives allows for fine-grained, automated control of the tool. For a partitioned approach and to support designs of unlimited size, Questa CDC supports hierarchical analysis with automatically generated CDC interface logic models (ILM).

## Questa Formal with AutoCheck

Questa Formal-based technologies also include Questa AutoCheck, which works directly on RTL to automatically synthesize assertions and perform formal sequential analysis. With AutoCheck, no testbench or user-written assertions are necessary. Questa Formal includes the industry's highest capacity property checking engines, which are tuned to handle large designs with large numbers of assertions, so they are particularly well suited for assertion synthesis applications.



*The Questa Platform provides a comprehensive SoC verification solution. The platform includes an array of verification capabilities seamlessly blending simulation and formal-based technologies with common compilation and user interface features, as well as the Unified Coverage Database (UCDB).*

**For the latest product information, call us or visit: [www.mentor.com/fv](http://www.mentor.com/fv)**

©2012 Mentor Graphics Corporation, all rights reserved. This document contains information that is proprietary to Mentor Graphics Corporation and may be duplicated in whole or in part by the original recipient for internal business purposes only, provided that this entire notice appears in all copies. In accepting this document, the recipient agrees to make every reasonable effort to prevent unauthorized use of this information. All trademarks mentioned in this document are the trademarks of their respective owners.

**Corporate Headquarters**  
Mentor Graphics Corporation  
8005 SW Boeckman Road  
Wilsonville, OR 97070-7777  
Phone: 503.685.7000  
Fax: 503.685.1204

**Silicon Valley**  
Mentor Graphics Corporation  
46871 Bayside Parkway  
Fremont, CA 94538 USA  
Phone: 510.354.7400  
Fax: 510.354.7467

**Europe**  
Mentor Graphics  
Deutschland GmbH  
Arnulfstrasse 201  
80634 Munich  
Germany  
Phone: +49.89.57096.0  
Fax: +49.89.57096.400

**Pacific Rim**  
Mentor Graphics (Taiwan)  
Room 1001, 10F  
International Trade Building  
No. 333, Section 1, Keelung Road  
Taipei, Taiwan, ROC  
Phone: 886.2.87252000  
Fax: 886.2.27576027

**Japan**  
Mentor Graphics Japan Co., Ltd.  
Gotenyama Garden  
7-35, Kita-Shinagawa 4-chome  
Shinagawa-Ku, Tokyo 140-0001  
Japan  
Phone: +81.3.5488.3033  
Fax: +81.3.5488.3004

**Sales and Product Information**  
Phone: 800.547.3000  
[sales\\_info@mentor.com](mailto:sales_info@mentor.com)

**North American Support Center**  
Phone: 800.547.4303

