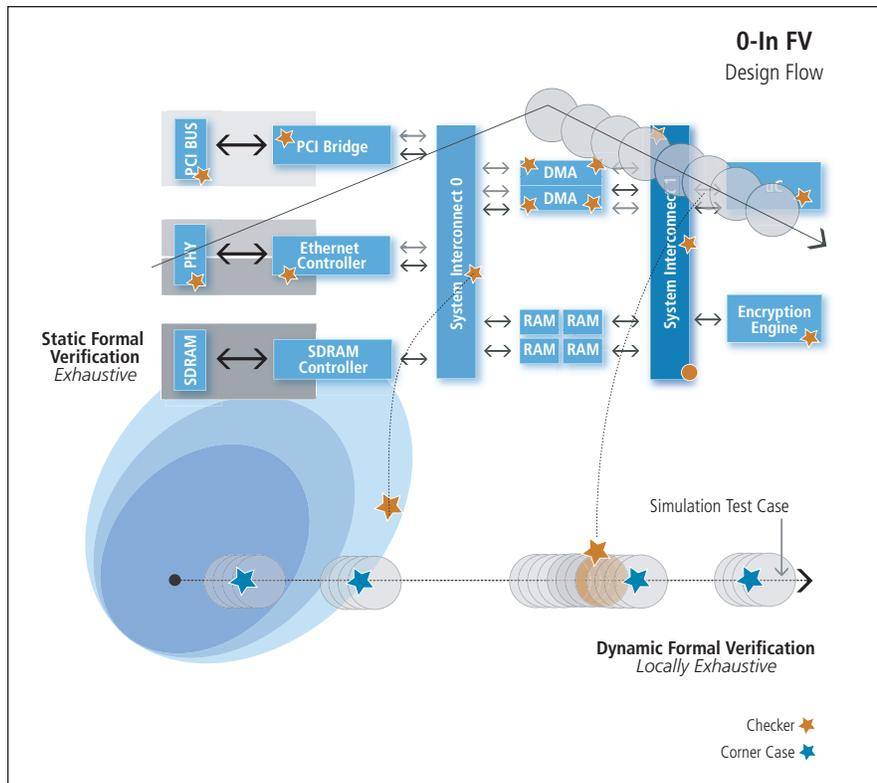


0-In Formal Verification



0-In Formal Verification combines static and dynamic formal technologies with simulation to provide the most powerful formal analysis in the industry.

Achieving Verification Closure Faster and Better

The Mentor Graphics 0-In® Formal Verification solution integrates the industry's most powerful static and dynamic formal verification technologies with the industry's most comprehensive assertion-based verification (ABV) solution, enabling users to achieve functional verification closure quickly and predictably. The 0-In Formal Verification solution is easy to use and provides value all the way through the design cycle — from block-level design, where it replaces traditional block-level simulation testbenches, to chip-level design, where it complements extensive pseudo-random simulation.

Target Tough Verification Problems

The 0-In Formal Verification solution delivers the most powerful, most comprehensive, and most widely deployed property-checking engines in the industry. Users can target complex logic with exhaustive analysis to increase confidence that corner-cases have been fully explored, and they can quickly and easily find bugs missed by traditional methodologies.

Major product features:

- Incorporates the industry's most powerful, highest-capacity, formal verification technology
- Uses static formal verification to exhaustively verify block-level designs without the need for simulation
- Uses dynamic formal verification to leverage chip-level simulation to find corner-case bugs
- Supports all standard assertion formats and libraries, including SVA, PSL, OVL, QVL, and 0-In CheckerWare®
- Supports comprehensive formal coverage metrics to guide verification
- Includes complete assertion-management system to analyze verification results, debug errors, and track progress
- Supports easy-to-use assertion-based methodology for specifying and debugging input assumptions
- Supports multiple clocks, gated clocks, memories, latches, X semantics, and non-synthesizable constructs
- Automatically reproduces assertion violations using an existing simulator

Tough verification problems ideally suited for the 0-In Formal Verification solution include:

- Standard-interface protocols
- Data integrity
- Arbitration logic
- Exhaustive block-level analysis
- Elasticity buffers and flow control logic

Integrated with Easy-to-Use ABV Methodology

The 0-In Formal Verification solution is tightly integrated with Mentor’s complete ABV solution. The designer or verification engineer can specify an assertion once and then use it without modification in simulation, formal verification, and emulation.

The 0-In Formal Verification solution allows all engineers to be productive with formal verification tools, enabling them to find bugs quicker and find bugs missed by simulation alone. The 0-In Formal Verification solution, provides key capabilities that make the use of assertions more efficient and effective:

- Powerful set of exhaustive formal verification engines
 - Static formal analysis, providing exhaustive proofs and counterexamples
 - Dynamic formal analysis, leveraging simulation to formally analyze critical corner-cases
 - Largest capacity formal analysis engines in the industry
 - Extensive design-style support
- Full support for standard assertion languages and libraries
 - SystemVerilog assertions (SVA)
 - Property Specification Language (PSL)
 - Open Verification Library (OVL)
 - Questa Verification Library (QVL)
 - 0-In CheckerWare®
- Complete assertion-management system to track verification progress
 - Assertion browser
 - Assertion violation browser
 - Total coverage viewer
 - Regression analysis
- Simple use model
 - Easy-to-use constraint (input assumption) methodology using assertions and CheckerWare
 - Ready-to-use, pre-verified formal constraints for standard bus interfaces
 - Detailed coverage information spanning simulation and formal analysis
 - Ability to fine-tune formal engines for “power-users”

Industry’s Most Advanced Formal Engines

The 0-In Formal Verification solution incorporates multiple, highly-tuned, modern, formal algorithms, including static and dynamic formal verification. The resulting formal analysis is the fastest and deepest in the industry. Static formal analysis is commonly used at the block-level to verify properties exhaustively. Dynamic formal analysis is commonly used at the chip level. Dynamic formal analysis leverages simulation by monitoring corner-case activity highlighted by assertions embedded in the design. It then focuses exhaustive formal analysis around these corner-case states, finding design bugs that would otherwise be missed. Together, dynamic formal and static formal verification complement a directed or constrained-random simulation methodology, providing more effective verification power to engineers and reducing the time to verification closure.

The 0-In formal verification engines automatically handle the broad range of constructs that are common in today’s designs, including multiple clocks, gated clocks, memories, latches, and X/Z semantics. They are tuned to handle large numbers of assertions, yielding the highest performance in the industry.

Best-in-Class Standards Support and Interoperability

The 0-In Formal Verification solution provides the most extensive support for standard assertion languages and libraries in the industry. Users are free to choose their assertion format, whether it is a language such as PSL or SVA, a library of pre-verified assertions, or a combination of the two. High verification productivity is achieved by using exactly the same assertions in simulation and formal verification.

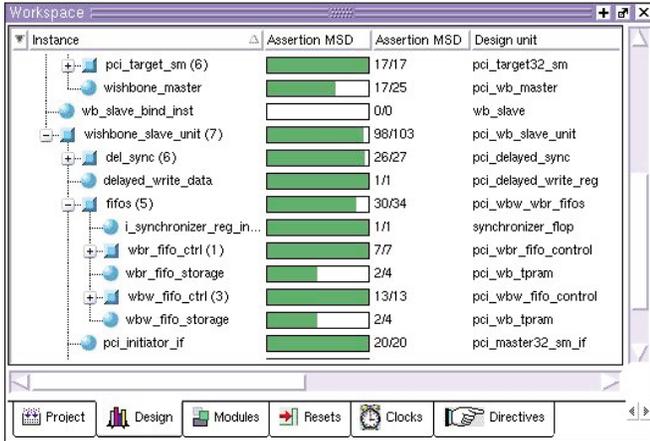
Comprehensive Library of Verification IP

By using either the QVL or the 0-In CheckerWare Library, designers quickly tap into the power of formal verification. The 0-In Formal Verification solution is completely compatible with these libraries, which includes a wide range of pre-verified elements for verifying common RTL structures (e.g., handshaking, FIFOs, arbiters, and FSMs) and standard interfaces (e.g., DDR-SDRAM, AMBA, and PCI Express). Each library element can be used either as an assertion to be verified or as an input assumption.

Comprehensive Formal Coverage Metrics

Even though formal verification analysis is exhaustive, users of formal verification tools need feedback to help them answer the questions: “Am I done?” and “What should I do next?” The 0-In Formal Verification solution provides the industry’s most comprehensive formal coverage metrics and methodologies to help answer these questions.

The 0-In Formal Verification solution reports a *proof radius* for each assertion, meaning that violation of the assertion is impossible within proof radius number of cycles. Typically, an infinite *proof radius* is reported for many assertions. For the remaining assertions, the *proof radius* number can be used to determine whether additional formal analysis is worthwhile. The 0-In Formal Verification solution supports direct targeting of assertion corner cases and preconditions using formal analysis.



Example of a structural coverage report.

The 0-In solution also offers *structural coverage* reports that can be used to find holes in the formal analysis test plan (e.g., an additional value needed in a configuration register) and to guide test plan improvements. All the coverage information can be exported to the Questa® Universal Coverage Database (UCDB), providing designers a single point of access for all coverage information, whether it originates from formal verification or simulation-based verification.

Easy-to-Use Methodology for Input Assumptions

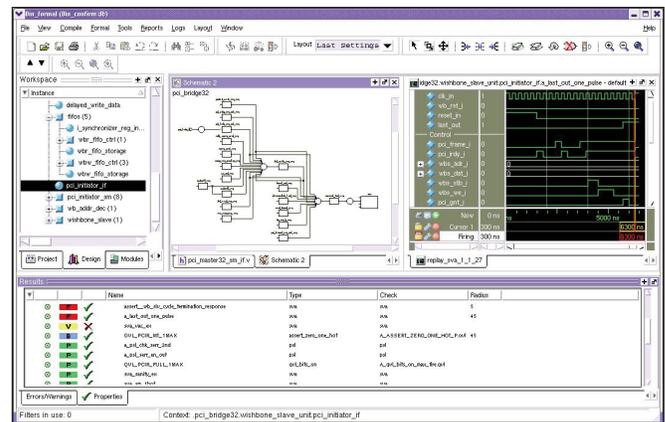
All formal analysis tools require that the user specify assumptions about the behavior of inputs on the boundary of the design; otherwise, assertion violations found by formal analysis may correspond to illegal input behavior instead of real bugs. The 0-In Formal Verification solution supports the

industry's easiest-to-use methodology for specifying and managing design-boundary assumptions. Design-boundary assumptions are specified at the block or cluster level, using assertions in any standard format or language. These boundary assertions operate during normal simulation runs, and any problems with the assertions can be easily diagnosed using simulation. When blocks or clusters are being integrated, the boundary assertions directly detect inter-block communication problems, substantially accelerating the verification process. The boundary assertions are used by formal analysis ensure that any assertion violations found represent real bugs.

Powerful Analysis and Debug

0-In Formal's dedicated GUI allows efficient control, analysis, and debug of the assertions and design being verified. It supports highly effective source code annotation as well as structural and waveform views to help designers understand results faster and identify the root causes of problems.

When 0-In Formal finds an assertion violation, it creates a testbench that enables an existing simulator to replay the scenario that produced the violation. This allows engineers to fully leverage their simulation debug tools, as well as the 0-In Formal GUI, to diagnose problems. A flexible, script-based control interface enables the inclusion of 0-In Formal into any regression environment.



0-In Formal offers an intuitive analysis and debugging environment.

Visit our web site at www.mentor.com/products/fv/abv/0-in for more information.

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