

Questa is a high-productivity verification platform featuring advanced verification technology designed to achieve coverage goals faster, reduce time-to-debug, and provide efficient and effective management of the verification process.

High-Performance Verification Environment

The complexity of today’s designs requires advanced verification technologies to maximize the value of each verification cycle and fast, high-capacity solutions to deliver the cycles for achieving sign-off coverage. Design complexity translates to complexity in the verification process as verification generates more data than can be managed using ad hoc methods. When verification successfully uncovers bugs, visualization of results at multiple levels of abstraction and automated debugging are required to speed the identification of root causes.

The Questa® verification platform delivers the full value of advanced verification and debug technologies within a comprehensive verification solution based on a metrics-driven verification management system. Questa spans the levels of abstraction required for complex SoC design and verification. Questa significantly increases the productivity and predictability of any verification methodology while improving design quality as well as visibility and control of the verification process.

Major product features:

- Leading support of standards: SystemVerilog, SystemC, VHDL, Verilog, PSL, UPF and C/C++
- Industry’s best integrated debug environment supports multi-abstraction debug and analysis
- Complete coverage support with assertions, code, and functional coverage for metric-driven verification closure
- Verification Management adds predictability by tracking coverage results against a test plan to optimize the design validation process
- Questa Power Aware Simulation verifies low power designs with Unified Power Format (UPF)
- Integrates with Questa Multi-View Verification Components (MVC), inFact™, Questa Codelink™, and Questa ADMS™ for complete electronic system verification

Open Verification Methodology

Through comprehensive support of advanced verification capabilities and industry standards, Questa enables the adoption of the open source, standards-based Open Verification Methodology (OVM). OVM is a base class library, utilities, and applications with a well-defined methodology for constructing verification components and testbenches. For more information see www.ovmworld.com.

Through the single-kernel, mixed-language environment provided by Questa, the OVM testbench can be connected to designs in Verilog, VHDL, SystemVerilog, SystemC, or any combination thereof. This flexibility allows all SystemVerilog verification environments, such as OVM, to be used with any design.

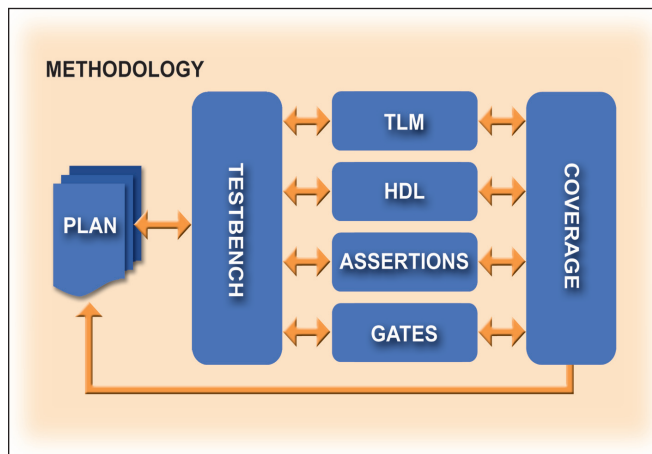
Adopting OVM with Questa closes the chasms between system designers, architects, RTL designers, and verification engineers. It facilitates the design and verification flow from system design to gate-level verification by maintaining the majority of the verification environment at the transaction level while providing abstraction adapters (aka drivers) to translate from the transaction to register transfer and gate levels.

OVM uses *sequences* to provide powerful constrained-random stimulus generation and a *factory* to configure tests in an easy, flexible manner. Factories create all verification objects, such as sequences and transactions. Questa recognizes OVM objects as part of the overall simulation hierarchy and supports the logging and viewing of transactions to facilitate debugging at the transaction level.

Test Automation

Questa verification features enable the automatic creation of complex, input-stimulus combinations that are extremely time-consuming to create manually. Stimulus scenarios can be described in terms of constraints using SystemVerilog and SystemC Verification library constructs. These constrained-random features help promote reuse at the testbench level, thereby reducing the number of testbenches that need to be written while increasing the amount of tests generated, bugs exposed, and verification coverage achieved.

The Questa constrained-random solver employs a variety of powerful heuristics to deliver high-quality sequences of random values efficiently, ensuring high coverage levels. The random nature of constrained-random testing allows the generation of stimuli and scenarios that may not have otherwise been considered, increasing the likelihood that bugs will be uncovered.



With native support of assertions, constraints, and functional coverage, Questa enables an optimized verification flow that fosters verification predictability and design quality.

Questa combines functional coverage with constrained-random testing to identify the functionality exercised by the automatically generated stimulus. Using functional coverage metrics as feedback for test creation, engineers can adjust constraints to focus random testing on coverage holes. This automation methodology offers huge productivity improvements compared to handcrafting hundreds of directed tests. Functional coverage metrics are provided through SystemVerilog coverage models (*covergroups* and *coverpoints*) and assertion languages (either SystemVerilog or Property Specification Language [PSL] assertions and cover directives). Furthermore, testbenches are able to react dynamically to functional coverage points in the design as the functional coverage data recorded in the Unified Coverage DataBase (UCDB) is available in real-time within the testbench.

inFact Intelligent Testbench Automation

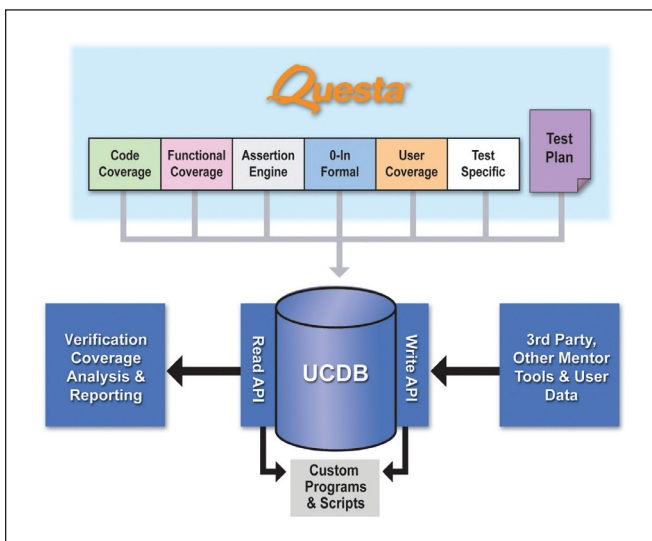
Questa integrates with Mentor Graphics' intelligent testbench automation solution — *inFact*. Although constrained-random stimulus generation achieves productivity gains by automatically generating tests, its random nature results in inherent redundancies as some test sequences inevitably replicate previously generated sequences. *inFact* algorithmically generates sequences, monitors results, and ensures generation of unique sequences. By eliminating the redundancies, Questa with *inFact* reaches coverage goals faster. *inFact* provides plug-and-play interoperability with OVM compliant verification components, allowing easy configuration of constrained-random or *inFact* tests. Please see the separate *inFact* datasheet at www.mentor.com/products/fv.

Verification Management

The application of constrained-random stimulus and metrics-driven verification dramatically increases the amount of data generated in the verification process. Questa was the first verification solution to collect all coverage data — code coverage, assertions, formal, and functional coverage — into a single UCDB. Questa’s UCDB stores coverage data and user-defined attributes, test data, etc. in a highly efficient format. Verification Management analyzes the coverage and verification data providing up-to-date information on the status of verification and insight on how to improve the efficiency and effectiveness of the verification process.

Verification Management imports verification plans and correlates coverage to test plan objectives, delivering a powerful tool for managers and engineers to continuously track progress and efficiently deploy resources against plan, providing a level of process visibility formerly unavailable. Verification managers can easily identify when specific areas of the plan are on-target or not. By associating priorities and weightings to plan objectives, the relative impacts of being on or behind schedule inform difficult choices over the course of a project.

Verification Management provides powerful analysis utilities that process the raw coverage data into actionable information. For example, a fully flexible test ranking capability provides the ability to identify redundant tests, sets of tests that achieve the highest coverage within a given amount of simulation time, or sets of tests that hit coverage points related to a functional area of interest.



Questa 6.5 Verification Management informs users when verification coverage goals are achieved. Integrated tools merge, analyze, and report all coverage data from multiple tools in a single database.

Because many verification flows incorporate tools from multiple vendors, and verification analysis metrics may be project or organization specific, an open and public read-and-write API to the UCDB provides the ability to integrate any verification tool into the overall metrics-driven verification process. Coverage data from proprietary and third-party tools can be inserted into the UCDB through the write API. Custom, proprietary analysis algorithms and reporting capabilities can be built on top of the read API.

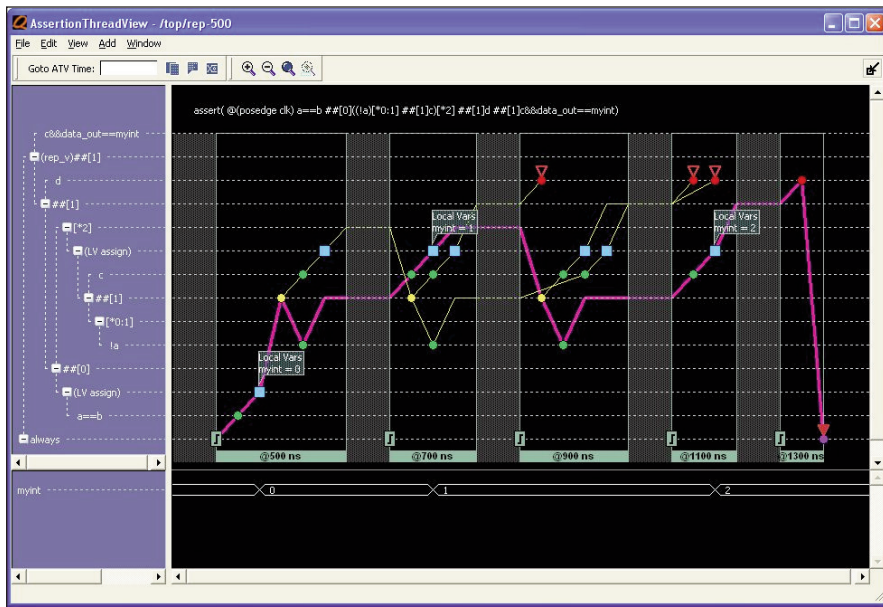
Assertion-Based Verification

Assertion-based verification (ABV) improves observability, detecting more bugs by using multiple “checkers” to monitor design behavior. It speeds time-to-debug by starting causality trace back at the assertion failure, which is at or significantly closer to the cause than are primary outputs.

Questa delivers a comprehensive standards-based ABV solution, offering the choice of SystemVerilog, PSL, or both. To ease the adoption of ABV, the Questa Verification Library (QVL) provides an extensive set of common RTL checkers — including the Accellera OVL checkers — and monitors for standard protocols; including AMBA AHB, AXI, OCP, PCI-EXPRESS, USB, and Ethernet. With the QVL, designers and verification engineers can realize the benefits of ABV without becoming an expert on property languages. QVL checkers and monitors are also supported by the Mentor Graphics 0-In® Formal Verification tool. In addition to predefined checkers and monitors in the QVL, Questa supports SystemVerilog Assertions (SVA) and VHDL assertions. SVA may be used through the SystemVerilog bind capability with SystemVerilog, VHDL, and SystemC components.

Questa’s debug capabilities integrate with assertions in multiple ways. Assertions may be logged and viewed in the wave window, indicating when an assertion is active, has passed or failed, and how many evaluation threads were activated for each evaluation of an assertion. The assertion browser provides statistical and status information on the number of activations, successes, and failures. When an assertion fails, Questa identifies the event that most likely caused the failure and directly traces the offending signal back to the source code.

The Assertion Thread View (ATV) window provides unique capabilities in debugging the cause of an assertion failure. The ATV visually shows the evaluation progress of all threads for a given activation of an assertion. The success or failure of the assertion depends on the success or failure of all threads spawned during the evaluation of the assertion.



The ATV window provides full assertion evaluation debugging.

The ATV shows each thread activation and its success or failure. Each failure is correlated back to the sub-expression of the property that failed.

Assertions provide functional coverage information that is automatically recorded in the UCDB, Questa integrates ABV with Verification Management. Assertion coverage can be the metric used to indicate whether or not a specific verification plan objective has been achieved.

High Performance

The foundation of Questa's industry-leading performance and capacity is its natively compiled, multi-language, single kernel architecture. Questa's high-performance global optimization mode, known as *vopt*, engages very aggressive compile and simulation optimization algorithms for all languages. *vopt* performance mode can improve Verilog/SystemVerilog and mixed VHDL RTL simulation performance by up to 6X. The *vopt* flow can also improve gate-level performance by up to 4X and capacity by over 2X. Questa utilizes multicore hardware with threaded waveform logging, introduced in May 2007, and threaded SystemC compilation, introduced in June 2008.

Questa also supports fast turn-around time to next simulation while maintaining high performance with the unique ability to pre-optimize reusable portions of a simulation. This is known as *bbox*. When a significant portion of the simulation is stable from one simulation run to the next, such as the design under verification, but other parts of the simulation change from one run to the next, such as the testbench or portions of it, *bbox* can be used to compile a fully optimized

version of the stable portion of the simulation while the mutable portion is compiled separately. *Bbox* provides the ideal trade-off between simulation turn-around-time and maximum simulation performance. Furthermore, since the *bbox* portion is reused, there are also significant disk space savings.

Power Aware Verification

Power management is critical for many applications. The techniques required to manage power present unique design and verification challenges. In response to customer requests for a better way to verify low power designs at the RTL, Mentor Graphics pioneered power-aware simulation.

Questa's Power Aware Simulation (PASim) is based on the Accellera-standard Unified Power Format (UPF), which was defined using technical donations from Mentor Graphics. The UPF provides a portable format for capturing low power design intent. Questa PASim combines the UPF specification with the HDL testbench and design description to accurately verify low power designs. PASim understands how the power network is constructed and connected to the design logic. It applies corruption (power-down) behavior when the supply to a power domain is shut-down, corrupt-on-activity behavior when a power domain is in a non-operational bias mode, isolation logic functionality for ports on power domains, and retention capabilities to registers as defined by the UPF specification.

Questa's PASim provides the industry's only capability to accurately model retention register behavior. The relationship of save and restore retention functionality relative to other operational register controls, such as reset and clock, differ widely from one technology library to another, even across technology nodes for the same silicon foundry. Verification of a low power design's power down and up sequence is incomplete or incorrect if generic retention register behavior is used. PASim supports behavioral descriptions of retention register functionality, ensuring simulation results match hardware behavior. With PASim, simulation results ensure that the design's low power management techniques are designed and implemented correctly for the targeted implementation technology.

Integrated Multi-Language Debugging

The Questa debug environment fully supports all standard languages and its GUI usage model is consistent across all

languages and abstraction levels. Questa automatically recognizes key objects in the design and verification environment, providing intuitive ways to view and debug these objects. For example, finite state machines (FSM) are inferred during analysis, and an FSM debug window provides a natural way to visualize the current state and state transitions of the FSM over time.

Questa also has best-in-class SystemVerilog debugging capabilities, including class contents and property viewing, and a watch window for gathering dynamic and static objects together in one place. Waveform viewing enables analysis of dynamic objects over time. Verification environments that are constructed with the OVM class library are recognized as part of the overall simulation hierarchy, even though the components of the verification environment are dynamic class objects. Questa manages the OVM hierarchy and transactions automatically.

Questa helps automate the often time-consuming and tedious process of tracing causality from an observed error to the root cause of the bug. Through either graphical or source based dataflow, the source and sink (driver and reader) relationships can be easily traversed to identify the origin of a bug.

Questa Multi-View Verification Components

Questa Multi-View Verification Components (MVC) is a library of verification components for common, standard bus interfaces. Questa MVC provides multi-abstraction views and interfaces covering all transaction level, RTL, and gate level interfaces. Questa MVC can be simultaneously connected to multiple components at any abstraction

level. The MVC abstraction adapter automatically converts between abstraction levels. Questa MVC components are compatible with the OVM and with a verification test plan to utilize Questa Verification Management. It provides constrained-random stimulus, monitors, and scoreboard/analysis capabilities.

When the optional MVCs are used with Questa, the MVC protocol recognition capabilities are fully exploited through visual association of the protocol stack from transactions to the RTL/gate signals that participate in the transaction. This helps speed the recognition of errors and the corresponding identification of the cause. Please see the separate Questa MVC datasheet at www.mentor.com/products/fv.

Questa Codelink and Questa ADMS

Questa Codelink provides the ability to perform processor based verification of SoCs with a single debug and control environment for both the software tests and the hardware being simulated and tested. The Questa ADMS simulator gives designers a comprehensive environment for verifying complex analog/mixed-signal SoC designs.

Please see the Questa Codelink and Questa ADMS datasheets at www.mentor.com/products/fv.

Platforms Supported

Questa supports: Linux 32-bit and 64-bit, Solaris 32-bit and 64-bit, Windows XP 32-bit, and Windows Vista 32-bit.

Visit our web site at www.mentor.com/fv for the latest product news.

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