

Mentor's 0-In CDC Powers Comprehensive CDC Verification at AMCC

On their very first project to use a comprehensive clock domain crossing (CDC) verification methodology, AMCC immediately achieved excellent results with the benefit of 0-In CDC's friendly use model and all around usability. On the spot support, compatibility with Verilog2000, good run times, and both structural and formal CDC verification capabilities contributed significantly to AMCC's confidence that their multi-clock SoC blocks are free of design killing CDC violations.

From its base in Sunnyvale, California, Applied Micro Circuits Corporation (AMCC) is a global leader in network and embedded PowerPC processor, optical transport, and storage technologies. The company blends systems and software expertise with high-performance, high-bandwidth silicon integration to deliver silicon, hardware and software solutions for global wide area networks (WAN), embedded applications such as PowerPC and programmable SoC architectures, storage area networks (SAN), and high-growth storage markets such as Serial ATA (SATA) RAID.

Founded in 1979, AMCC has been the market share leader in packet processors since the inception of the network processing industry. Its award-winning PowerPC® processors use best-in-class-technology and have achieved mass-market acceptance from major networking, storage, and consumer OEMs.

A recent high-performance network processor presented a new challenge for the AMCC team. The network processor consisted of two principal parts: a PowerPC embedded processor core and a multi-clock domain SoC that includes Ethernet and other standard interfaces. Both parts required CDC verification, but the SoC was more challenging because of the complexity of its clock domains and the signals that pass between them. The SoC was made up of ten interconnected blocks, approximately 100 memories, a variety of third-party IP, and about two million standard cell instances. The number of clock domains on each individual block ranged from three on the simplest to an astounding 42 on the most complex.

Obviously, they had a truly complex and complicated clocking scheme on their hands. It was clear to the AMCC team that this design required a CDC verification solution both more sophisticated and more comprehensive than anything they had used before.

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KARL PFALZER
CHIEF VERIFICATION ENGINEER
AMCC



After 20 years of engineering, Karl Pfalzer still finds inspiration in the verification and implementation puzzles he has to solve to deliver complex ICs.

Fortunately, Mentor Graphics® 0-In® CDC tool's usage model, performance, and technical support made it easy for AMCC to successfully unravel this intricately tangled and seemingly intractable problem.

Synchronizing Watches Automagically

The drastic increase in the number of asynchronous clock domains on many of today's chips makes the manual review of all the crossings in a design impractical and highly error prone. Only a comprehensive solution for CDC verification ensures that the appropriate synchronization structures are used throughout the design; that the protocols required for those structures are followed at all times; and that the design techniques applied to deal with all forms of reconvergence function correctly. Traditional verification techniques fail in all of these areas, making CDC problems a very high risk for design groups.

When Karl Pfalzer took up his duties as chief verification engineer of this AMCC team, the Mentor 0-In CDC tool was already part of their tool suite. However, in performing proper diligence, he evaluated competitive CDC verification tools before committing to 0-In CDC.

"CDC by nature is inherently a very difficult process and the tools can be difficult to use," explains Mr. Pfalzer. "There was some concern that the Mentor solution would also be difficult, so we checked out a few other vendors. We came back to Mentor for the reason

of usability. Compared to other vendors, we were very pleased with the solution and already look forward to using it for future projects."

As this was the first project where AMCC wanted to perform CDC verification at the block level and then at the full chip level, there was a lot for them to learn and many new things they had to face along the way. Fortunately, they

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had the benefit of Mentor's on-site and factory-based support—known for its responsiveness, technical savvy, and individualized service.

Throughout the project, when the AMCC team hit the inevitable snag, such as minor problems with nuances in Verilog 2000, they found Mentor technical support to be both thorough and highly responsive.

"The support for this tool has been excellent," Mr. Pfalzer remarks. "I'll

fire an email to 0-In support and get fantastic turnaround times; on the last one, I got a response in five minutes. Sometimes it gets into some fairly involved examples, and I don't expect fast turnaround then, but I'll get a detailed analysis and results and explanations back."

But the team first got started with comprehensive training, given by a Mentor CDC expert, on the nature of CDC, its problems, and why a specialized tool is needed to address them. Mr. Pfalzer then worked with the Mentor specialist to set up an efficient, structural CDC verification flow for all ten blocks.

First, the CDC tool has to be given information about the clocks in the design. 0-In CDC automatically converts the designs RTL SDC file (which has all of the clock information used in the implementation) into its own dialect format. The resulting file can be modified, if necessary, to add extra information about, for example, different modes. From there on it's a fairly mechanical process. The tool generates the CDC database and spits out a brief summary report and a binary database that can be quickly loaded into the CDC tool to start using its visualization debugging functionality.

"For a problem like this you need excellent visualization techniques, and that's where the Mentor CDC tool definitely shines above the rest," Mr. Pfalzer observes. "The 0-In CDC use model is great. It outshines the others in terms of showing where the problems are, helping organize that information,

using familiar schematics and blocks, color-coding clock domains and crossings, and so forth—all of which help you iterate and successively refine. You're often surprised as a designer by the things a tool like this finds."

In other words, the familiar user interface makes a very complicated subject easier to understand and correct. It even tells the user whether they should worry about a problem at all.

"When 0-In CDC reports that something is wrong, its excellent GUI presents a very succinct view of the violation," Mr. Pfalzer continues. "It's got excellent schematic rendering capability, excellent navigation capability, and good color coding that distinguishes between severe, not so severe, and things you don't have to worry about initially."

The AMCC SoC has typical control-level synchronizers, which are pretty easy for structural checkers to find. However, it also includes very complex data crossings that require sophisticated, sequential data, stability checking technology.

"As we've been running through these sophisticated checks, we've been pleased with what the tool can do *automagically*, if you will, in terms of recognizing all the common structures," Mr. Pfalzer enthuses. "It's flagged some issues; including asynchronous resets and asynchronous crossings that forced us to look very closely at the structures we were using. There were also a few surprises that the tool correctly proved to indeed be wrong, so we had to

change some of those structures. Many designers underestimate the importance of this: if one of these CDC issues makes it to silicon, your chip is dead."

Progressing to Formal

Mr. Pfalzer was pleased to discover that 0-In CDC exceeded his original expectations regarding its structural verification performance, and he has begun running 0-In Formal on parts of the chip that have completed the structural phase of the CDC verification flow.

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"There are two phases to CDC verification: a structural phase and a formal phase," Mr. Pfalzer explains. "You can't start formal until you're pretty clean in the structural phase. I've run through some simple test cases and cobbled together a flow to simplify the movement from structural to formal. 0-In automatically recognizes as many as 28 structural CDC schemes and automatically generates the protocol checkers that formal operates on. We're just beginning to use it, but I already have confidence in what the tool is reporting and why it reports something is wrong.

At this point, I feel that our design is probably 80 percent CDC verified, and maybe 90 percent correct—another 10% is going to be resolved once we finish running the formal."

Mr. Pfalzer also looked into the formal capabilities of competitive tools. Again, he ended up coming back to 0-In CDC, as it turned out that the features they were looking for from the other vendors already existed in the Mentor tool.

"We didn't know that the Mentor tool had all the formal capabilities that it has," Mr. Pfalzer recalls. "These are crucial when you get into the more advanced kind of CDC checking. When I started using it for structural verification, it met my expectations. After I kicked the tires on a couple of other features, it exceeded my expectations and really stood out with respect to the competition."

Taking It to the Next Level

Ultimately, he plans to use 0-In CDC for top-level verification of the full network processor design. Furthermore, he would like to apply the tool earlier in the design flow, particularly to qualify IP from a CDC perspective.

"That's definitely one of the first things I would use it for," Mr. Pfalzer explains. "The other thing is, at this point our designers are convinced that it's easy enough to use, so we will certainly make it part of and use it very early in our design cycle. As soon as we have code that simulates what is actually in the ASIC, we will run CDC."

This is perhaps more of an achievement than it first appears, because Mr. Pfalzer initially faced resistance to adoption of the tool, chiefly because of fears the tool was difficult to use and because the importance of the CDC issue was not recognized. This has definitely changed at AMCC.

“Our designers are working with it now, they’re more accepting of it,” Mr. Pfalzer tells us. “If you give them this much information on a silver platter and make it easy for them to use the information, they’re more accepting. With Mentor’s assistance and the quality of the tool itself, we’ve made it much more accepted and easier to use.”

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