

Mitsubishi selects Mentor's hardware-assisted verification solutions – including Veloce for its next-generation HDTV video decoder IP

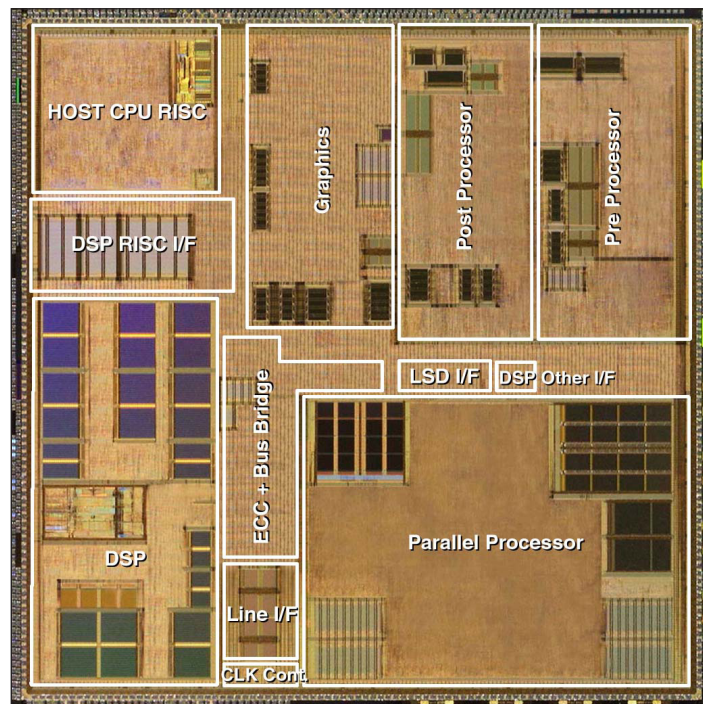
When Mitsubishi needed to rapidly verify its multi-mode multimedia communication processor, it adopted Mentor's hardware-assisted verification solutions. Today, Mitsubishi and Mentor are together again – this time using Veloce emulator – to help validate Mitsubishi's next-generation HDTV video decoder IP.

In the world of System-on-Chip (SoC) verification for multimedia devices, producing high-quality, first-pass silicon chips is critical to business success. Mitsubishi realized long ago that conventional methods of verification needed to be drastically improved to meet their business objectives. Because of increasing design capacity and time-to-market demands, verification by software simulation was no longer an option. Further, designs suited for multimedia applications seem to grow in complexity by the day, approaching a limit to the handling of gate complexity and verification performance with a software only solution.

Additionally, verification of Mitsubishi's chips increasingly require comprehensive application-level software testing with "live" stimulus to ensure efficient pre- and post-silicon debug.

Mitsubishi selects scalable methodology from accelerator to emulator

Mitsubishi required a comprehensive and high-performance solution for both acceleration and emulation in



*Mitsubishi's
Multimedia
communication
LSI.*

order to develop Multimedia communication LSI, and selected Mentor's hardware-assisted verification solutions as a result. The company knew that software simulation would be inadequate to obtain the testing coverage required for its recent high-complexity chip. What was required was tremendous speed and high-performance capabilities of an emulator that could perform verification within an acceptable time frame.

Mitsubishi uses a bottom-up approach to their verification; from block level to chip level, and finally to system level. This provides an effective and reliable methodology for the company. Mitsubishi utilizes multiple applications within the emulator for acceleration and finishes with in-circuit emulation (ICE). This methodical, step-by-step approach delivers the reliability and efficiency Mitsubishi seeks in an overall verification program. Mentor's

hardware-assisted verification platform plays perfectly into what Mitsubishi requires.

Verification methodology used by Mitsubishi

Mitsubishi used the following emulation methodologies, step by step, through their bottom-up approach and applied it to their designs:

1. Co-simulation with a software simulator.
2. Mapped designs to be verified and the testbench to the emulator; then verified them with actual video data.
3. Finally, IPs without RTL models are mounted on an external board to connect with the main board – total system is then verified with ICE.

Mentor Graphics hardware-assisted verification solutions provided a flexible verification capability at each verification phase, delivering on the high-performance requirements Mitsubishi demanded.

In-circuit emulation also key to verification success

Because Mitsubishi was able to tap into Mentor's ICE capabilities, the company performed a variety of unique verification techniques. For example, Mitsubishi was able to adopt ICE solutions for parts of their design (RISC processor and DSP) that were supplied by third-party vendors – for which the company had no RTL models. In this situation, Mitsubishi used the real device for each type of processor, and

built an external board that connected directly to the emulator. As a result, Mitsubishi had a vendor-certified and accurate representation of their processors in the design – and thus, were able to accelerate the verification.

Mentor's unique clock implementation capabilities put to task

Due to the nature of Mitsubishi's multimedia designs, there was a critical need for multiple clock domain handling – a capability Mentor's hardware-assisted verification platform is able to provide due to the inherent architecture of its emulation-on-chip.

mently; the software team would design, develop, and debug according to their own set of specifications and the hardware team would do the same – everyone worked in isolation.

The type of verification solution offered by Mentor not only brings these teams together, but allows engineers to work together earlier in the design process, saving time and catching bugs during block and chip verification rather than later in the pre-silicon prototyping stages of development.

Mentor's hardware-assisted verification solutions have proven to be very successful for Mitsubishi. So when the company had an even tougher chal-

“We decided to transition to Mentor's Veloce hardware-assisted verification platform due to better capacity in a smaller footprint, faster compile time, and MHz-class runtime.”

— NORIYUKI MINEGISHI, MITSUBISHI ELECTRIC CORP.

Mentor's hardware-assisted verification platform's flexibility and modeling accuracy allowed Mitsubishi to take advantage of real-world behavior and avoid risks of chip failure due to clock domain issues.

Perfect system verification

Mentor's hardware-assisted verification solution brings a new paradigm to how engineers verify, validate, and simulate their design. For so long, verification engineers worked indepen-

lence – verification of a multi-standard HDTV video decoder IP – Mitsubishi adopted Mentor's Veloce hardware-assisted verification platform.

Mitsubishi's complex, next-generation HDTV video decoder IP

Because the Veloce Solo can handle designs up to 16 million gates, capacity was more than adequate to verify the 1.5 million gate IP. The real challenge came in testing the functional complex-

ity of the three mandatory video standards specific to the Blu-ray application. These three corresponding video standards included; MPEG-2, H.264, and VC-1. Each in itself is a complex standard to test, but Veloce had to handle the tests in a real-world environment.

In addition to Veloce testing the functional complexity of the standard, there was also the issue of verification complexity. For example, H.264 requires ten times the computational

load of MPEG-2. Another key area was the sheer volume of verification tests. The DUT had to be tested at full HDTV mode (1920 x 1280) at 30 frames per second.

Early results look extremely promising

The HDTV video decoder emulation identified over 60 bugs in the first phase and eight more bugs in the second phase. Unquestionably, this

will help ensure first-pass RTL success. The use of Mentor's Veloce emulation-centric verification flow also helped Mitsubishi reduce hardware development time, allowed verification teams to run more verification cycles, which ultimately help to prevent tapeout delays and costly respins.

Mitsubishi joins a growing list of leading-edge customers who have successfully incorporated Veloce into their functional verification flow.

“We taped-out a design of a multi-standard HDTV video decoder using Veloce, so far the HDTV video decoder emulation identified over 60 bugs prior to tape-out, ensuring high quality of the RTL.”

— NORIYUKI MINEGISHI, MITSUBISHI ELECTRIC CORP.

Visit Mentor Graphics at www.mentor.com/emulation for additional product information.

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