

Questa OVM Helps SEAKR Dock a Verification Environment for Space Age FPGAs

Launched by Mentor Graphics' pragmatic and personalized training and support, SEAKR enjoyed a fast ramp up with not only new technologies but also a new focus. The ease of use of Questa's advanced verification technologies helped them quickly set up advanced testbenches that found more bugs and exercised more fully their customer's designs in record time. The ability to verify their designs better and faster while also providing a beneficial service to their customers landed SEAKR a larger revenue stream.

SEAKR is the leader in space-based, solid state storage and processing systems. With 200 employees, they are large enough to do everything in-house and maintain rigorous security, yet small enough to keep down the overhead costs that might tempt some companies to cut corners. From their 55,000 sq ft facility in Centennial, Colorado — custom designed and built to maintain a flow and efficiency that is consistent with the quality and handling standards of the aerospace industry — the engineers at SEAKR create data storage and processing systems for both manned and unmanned applications. Their data recorders and other products have been to the moon, visited Mars, and even touched down briefly on an asteroid. Their systems can also be found on the space shuttle and the international space station.

In the 1980's, the company's founders believed they could replace the aging tape recorders then utilized in space with solid state recorders—and

make them better, faster, cheaper, and longer lasting. Toward fulfilling this goal, SEAKR pioneered the use of plastic encapsulated memory (PEM) for storage systems. Knowing that PEMs will fail, SEAKR devised a means to mitigate the failure effect. In other words, SEAKR's designs center around the ability to test and correct errors associated with the effects of space. By

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**GREG BAKER
SENIOR DESIGN ENGINEER
SEAKR**



Nirav Patel, Craig Horn, Kelly Miller and Greg Baker.



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taking this new approach, SEAKR was able to fulfill their initial promise to provide products for the space community at a much lower, more competitive rate, faster than anyone.

Because of this unique expertise in FPGA and ASIC design, SEAKR was recently approached by an external customer to verify their designs. It was during these engagements that the SEAKR engineering team became a firm believer in the high value of assertions, advanced coverage features, and the Open Verification Methodology (OVM) as supported by Questa®. Questa made it easy for them to quickly set up complex test environments and use and reuse them to find unexpected, critical bugs and thoroughly exercise the designs.

“Using the constrained-random capabilities of Questa and the OVM,” explains Kelly Miller, Senior Hardware Engineer at SEAKR. “We were able to see much deeper into the design, come up with many different scenarios, and expose many different bugs.”

SEAKR found a number of issues related to the customer’s FPGA implementation that the customer’s internal verification activities had not uncovered. Their customer was so pleased with the speed and quality of the results that they upped their original contract for the verification of one design to three. Further, SEAKR was inspired to establish a full time verification team, separate from their design team, to verify both in-house and third party designs.

Setting a New Trajectory

However, when the customer originally approached them, this level of verification was new to them. To become proficient as quickly as possible and then expand their expertise, several members of the SEAKR verification team participated in the OVM and SystemVerilog classes provided by Mentor and its partners. They also had around ten lunch-and-learns, personally customized by their Mentor AE.

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**KELLY MILLER
SENIOR HARDWARE ENGINEER
SEAKR**

“We found the classes to be absolutely useful and worth the time to attend,” Mr. Miller says without hesitation. “On top of that, our AE has been coming in for tailor made lunch-and-learns. They are extremely valuable.”

In addition to training and regular visits by their AE, technical support was always a phone call away.

“Being able to call up our AE at a moment’s notice was really helpful in getting up and running,” recalls Jeff Pritchard SEAKR’s Technology

Director. “If I had any questions, I could just call him on his cell phone, and he would answer right away. Plus the tool was pretty seamless and easy to use.”

“We participate in Mentor’s web casts too,” adds Rich Groepper, another senior design engineer at SEAKR. “That’s another good way we get support.”

Accelerating Productivity

SEAKR further expanded their verification capabilities by hiring Craig Horn to work on an internal design effort. Mr. Horn was the first engineer dedicated solely to verification at SEAKR. His first project was a multi-FPGA, automated payload switch for the International Space Station, with one FPGA acting as a switch and another as a controller.

The switch had already undergone directed Verilog testing and some board testing as an FPGA prototype. Mr. Horn wanted to run more sophisticated tests on the FPGA. Starting with a small OVM example supplied by the Mentor Graphics AE, Mr. Horn was able to construct a self-checking constrained-random testbench within a few months.

“This was a much better experience than when I used constrained random at a different company using a different tool,” Mr. Horn observes. “The other tool was not as polished and not as easy to put together as the OVM. With the Mentor AE’s OVM code example and training, I had a robust testbench for the switch FPGA in a few months; the other tool would have taken six months.”



SEAKR's 55,000 sq ft facility in Centennial, Colorado was custom designed to maintain a flow and efficiency that is consistent with the quality and handling standards of the aerospace industry.

The OVM constrained-random testbench was able to expose issues with the prototype, finding corner cases that had not been anticipated. By using assertions on the outputs, Mr. Horn was able to locate a violation of the output traffic constraints and of other corner cases where packets were corrupted. These had not been exposed with either board or directed testing. In other words, Mr. Horn not only cut development time in half while learning a new methodology but also found critical bugs on a pre-verified design.

Mr. Horn gained an even greater productivity boost on the controller FPGA by taking the general structure of his first test environment and, with minor tweaks, expanding it to an environment that had four times the complexity, including many more interfaces that needed to be driven and checked.

“The speed with which you can construct the environment and the ease of expanding it to other applications are two major benefits,” Mr. Horn emphasizes. “Because of the object-oriented way that the OVM is set up, in two months I was able to expand the testbench that I had created for the switch to cover both the switch and the

controller FPGA. In fact, I was able to have that ready to start testing before the RTL for the controller FPGA was released. I’m very happy with that.”

Due to its multiple configurations, the verification space of the device was very large. Using constrained random and the OVM, Mr. Horn found it easy to achieve full coverage quickly; whereas with directed testing, his experience had been that it would be very hard to do this properly, if it could be done at all.

“It would have been very difficult to reach full coverage of the device with directed tests,” observes Mr. Horn.

“Due to the nature of constrained-random traffic and configuration, and the ease of extending the base classes, it’s very easy to have an environment that runs tests and automatically judges the results. It’s really a job at that point that one person can do.”

Boosting the Next Testbench

It was while Mr. Horn was still at work on his designs that the aforementioned customer approached SEAKR to verify the first of what turned out to be three FPGAs for satellite and payload environments. The chip was behind

schedule and the customer did not have the manpower or schedule to do the verification internally. Mr. Miller and Nirav Patel, a verification engineer at SEAKR, worked on-site with the customer’s designs.

After learning about the design, SEAKR came up with a test plan and a verification environment within about two weeks, and the first testbench and fully verified FPGA in one month. This rapid success was due to a combination of Questa’s ease-of-use and the quality of Mentor training and technical support.

“The ability to come up with an environment and test vectors and results in about a month was pretty impressive,” Mr. Miller remarks. “This included not only learning the customer’s product and how we needed to plan to test it, but also bringing up the environment and developing reference models. Pulling all of that together in that amount of time says a lot for the tool and its ease of use as well as the ease of use of the methodology.”

As a comparative study, Mr. Patel used a constrained-random testbench while Mr. Miller ran a directed test case environment on that same design. Although Mr. Miller describes his directed test suite as a very good one, the constrained-random environment found many more bugs.

“You can see right away that constrained random uncovers things that you would not have found using directed tests,” says Mr. Patel.”

Their client was so impressed with the bugs SEAKR found and the short amount of time required that they asked

them to perform third-party verification on two other FPGAs in the same product line. One of them had been completed for two years, was fully verified, and was ready to be programmed. The second was far into the design cycle and had been through some verification.

“Based on our success, our customer was able to recover some of their schedule,” explains Kurt Anderson, a Program Manager at SEAKR. “So they expanded our contract to the other two FPGAs of this product line. That’s an enormous value to us.”

The second FPGA addressed the analog functions on board the spacecraft, and the third was a general purpose FPGA that handled a number of different interface functions, command functions, and an execution function. They were able to reuse Mr. Horn’s OVM testbench to get fast, meaningful results.

“We used a lot of the work Craig did as a baseline for our work,” recalls Mr. Patel. “We had a transaction-based reference model and were using OVM and its capabilities, and we got that running and got results in less than a month.”

“One of the things I like about OVM is I can construct a fairly robust set of constrained tests with a very small configuration object,” Mr. Horn explains. “And by documenting that very carefully, other engineers can use my environment very easily without knowing what’s under the hood.”

Similarly, the modular aspect of the OVM also allowed SEAKR to divide the design among different members of a team.

“The tool is parsed up nicely enough to where you can bring in a second, third, or fourth person and give them different parts of the design to work on,” Mr. Miller explains. “And they only have to know that one little piece of the tool, yet it all comes together in the end as one verification environment.”

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**CRAIG HORN
VERIFICATION ENGINEER
SEAKR**

Like Mr. Horn, Mr. Miller’s team also used constrained-random stimulus to find unexpected scenarios. In one case, an operational effect could lock up the chip by sending in commands when it was not supposed to.

“This scenario only came up because of the constrained-random environment,” says Mr. Patel. “Normally when you create directed test cases, nobody would think to have this kind of scenario in it. As a result, we recommended a lock out feature, and our customer changed their design accordingly.”

“Questa definitely gives you a better way to find design defects,” adds senior design engineer Greg Baker. “With

constrained-random testing you can test things you hope would never come up. When you are putting a design up in orbit you can’t just walk down to the lab and hit the reset button when something goes wrong. You have to have it rock solid before you go. Finding this stuff before programming is a monstrous cost savings. I would guess we easily saved our customer more than the cost of our contract.”

They also found that OVM helped them in both their adoption of SystemVerilog and in getting the most out of its benefits. Questa’s coverage features were also indispensable in ensuring they had exhaustively verified their design.

“To get the full power of SystemVerilog you need a methodology, and OVM provides that,” observes Mr. Patel. “We used assertions in the interface, which were very useful. For example, we found three violations of the spec in one of the designs. Coverage is another feature we really needed. Sometimes it is very difficult to decide whether you are done with verification. Questa code and functional coverage metrics told us when all the coverage points were covered.”

Verification Management Is in the Stars

With their customers’ FPGAs well on their way to outer space, and their new third-party and in-house verification service successfully landed, SEAKR looks forward to other ways to augment their verification attack. They see verification management as an important facet of their next advance.

“One of our next steps is to incorporate the specification into the tool through verification management,” says Mr. Anderson. “Our customers have actually asked for it. They want to make sure every requirement has a test associated with it. By using this methodology, you can give the customer a much higher level of confidence that everything has been verified on the chip that is in their specification. Questa’s verification management feature is one more way of automating that output.”

“Sometimes we came up with our own requirements, even extending from the customer’s requirements,” Mr. Miller adds. “And we could plug those in as well. So not only can we cover their specs, but our derived specs as well.”

Taking Risk Out of Space

Using the many advanced verification techniques and methodologies made available by Questa, SEAKR has taken the next step in verification, moving from directed tests and proto-

types to a more sophisticated approach for improving design quality and verification productivity.

“Now we’re able to offer a new verification service to other companies,” observes Mr. Anderson. “Questa and the OVM are not only helping our designs, but we’re also able to provide a service to help other companies with their designs. It helps burn down risk up front. People very quickly see the value that’s added here.”

“With FPGAs and ASICs getting so big, complex, and expensive, with more and more functions, you want to make sure that you don’t have to spin that chip,” Mr. Anderson concludes. “You certainly don’t want to ship something to a customer and then find out there’s a mistake when it’s already bolted onto a payload. The better you can verify things upfront, the better it is for your bottom line. Questa enabled us to do that.”

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**NIRAV PATEL
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