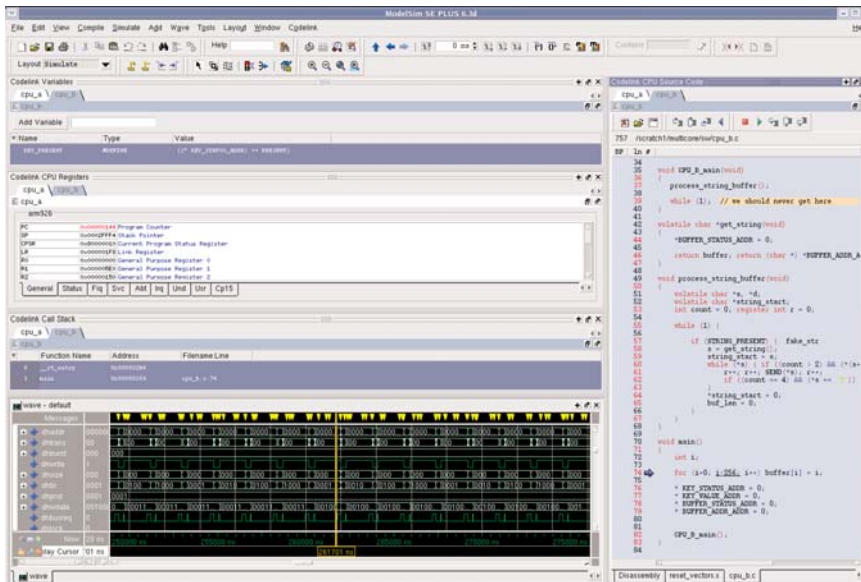


# Questa Codelink Advanced Functional Verification

D A T A S H E E T



Codelink features source-level debug for RTL processor models. Source, SW variable, register, memory, and call stack windows are supported for multiple processors.

## Overview

Questa Codelink delivers source-level debug for code executing on RTL processor models from ARM and MIPS. Connecting to your existing RTL model in read-only mode, Codelink has no impact on simulation results. Patent-pending technology transforms general purpose register info into a rich source-code debug environment. Isolate the cause of processor-driven test failures in a fraction of the time it takes using text files and waveforms. Codelink logs register state info during a run so you can debug post-simulation. There's no need to rerun time consuming batch runs in order to isolate the cause of failure.

## Debugging Processor Driven Tests

Let's face it. Logic simulators aren't designed for software debug. Staring at waveforms and sifting through instruction traces and symbol tables is frustrating and time consuming. That's why we developed Questa Codelink. Codelink monitors the register changes of RTL processor models from ARM and MIPS and creates a rich software debug environment.

Set break points; step through code; view variables, registers, memory, and the call stack. Codelink is fully synchronized with logic simulation and tracks the position in the source window as you drag the waveform cursor around.

## Major Product Features:

- Source-level debug for ARM and MIPS RTL processor models
- Multi-core support
- Source, assembly, memory, variable, register and call-stack views
- Logs processor registers during simulation and synthesizes complete dataset for interactive post-simulation debug
- Step forward or backward through source or assembly
- Code and Wave windows are fully synchronized
- Connects to existing RTL processor models
- No design or model changes
- Zero impact to simulation results and accuracy

## Major Product Benefits:

- Isolate processor driven test failures in minutes
- Replay overnight simulations in seconds
- Easily attaches to ModelSim or Questa simulations
- Debug multi-core synchronization errors
- Eliminate static symbol table and assembly listings
- Dramatically reduce debug time for processor-driven tests

## Interactive Post-Simulation Debug

There's no need to re-run failing regression tests in order to isolate the cause of failure. During simulation, Codelink logs processor register and memory state changes. Post simulation Codelink loads a software log-file in conjunction with the waveform log-file so you can enjoy interactive HW/SW debug. How interactive? Codelink can replay a 15-hour simulation from start to finish in just 3 seconds. You can move instantly to any point in the simulation record with full debug visibility. You can also debug during simulation if you prefer.

## Step Through Code in Reverse

Codelink has the ability to un-execute code so you can step backward through C or assembly. This is a critical feature for pinpointing the cause of a failure. Stepping forward and back through a suspect code segment quickly pinpoints the errant statement. As you step, a cursor in the Wave window simultaneously tracks your position. You can also drag the Wave cursor to a suspect transition while the source window points to the corresponding code.

## Multi-Core Support

For multi-core designs, Codelink simultaneously monitors multiple processors. Any mix of supported processors can be logged during a single simulation. The Questa Codelink debugger presents source, memory, register, variable, and call stack windows for each core in the design. The user can choose tabbed, tiled, vertical, or horizontal window orientation.

## Easy Setup, Identical Simulation Results

Running Codelink is as simple as adding a switch option to your Questa or ModelSim invocation, then specifying the path to the processor model(s) you want to debug and the location of the ELF file directory(s). Because Codelink

simply observes the registers of your existing RTL processor model, it has zero impact on your simulation results. There's no need to change any of your simulation models or your test bench. You don't even have to recompile your code, even though for the best debug experience compiling without optimization is recommended. Codelink logging overhead is less than 1% of total simulation time and the software log-file is a fraction of the size of a typical waveform log or VCD file.

## Supported Processors

Questa Codelink supports most ARM and MIPS cores. Codelink connects to the vendor-supplied, RTL-based processor model. It works with both RTL and VMC-compiled RTL processor representations. Supported cores include:

	ARM	MIPS
7tdmi	1176jz(f)-s	4KE
7tdmi-s	11 MPCore	M4K
926ej-s	Cortex-M3	24K
946e-s	Cortex-R4	74K
968e-s	Cortex-A8	

## An Integral Component of Questa

The Questa advanced functional verification environment combines high performance and high capacity with the most comprehensive verification capabilities in the industry. Questa works with any design and verification flow, incorporates best-in-class technologies, and spans the levels of abstraction required for complex SoC design and verification. Questa significantly increases the productivity and predictability of any verification methodology while improving design quality, equipping design and verification teams to meet schedules and attain maximum design functionality.

Visit our web site at [www.mentor.com/codelink](http://www.mentor.com/codelink) for the latest product news.

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**Corporate Headquarters**  
Mentor Graphics Corporation  
8005 SW Boeckman Road  
Wilsonville, OR 97070-7777  
Phone: 503-685-7000

**Sales and Product Information**  
Phone: 800-547-3000  
503-685-8000

**Silicon Valley Headquarters**  
Mentor Graphics Corporation  
1001 Ridder Park Drive  
San Jose, California 95131 USA  
Phone: 408-436-1500  
Fax: 408-436-1501

**North American Support Center**  
Phone: 800-547-4303

**Europe Headquarters**  
Mentor Graphics Corporation  
Arnulfstrasse 201  
80634 Munich  
Germany  
Phone: 49 (0) 89 57096-0  
Fax: 49 (0) 89 57096-400

**Pacific Rim Headquarters**  
Mentor Graphics (Taiwan)  
Room 1603, 16F  
International Trade Building  
No. 333, Section 1, Keelung Road  
Taipei, Taiwan, ROC  
Phone: 886-2-87252000  
Fax: 886-2-27576027

**Japan Headquarters**  
Mentor Graphics Japan Co., Ltd.  
Gotenyama Hills  
7-35, Kita-Shinagawa 4-chome  
Shinagawa-Ku, Tokyo 140  
Japan  
Phone: 81-3-5488-3030  
Fax: 81-3-5488-3021

