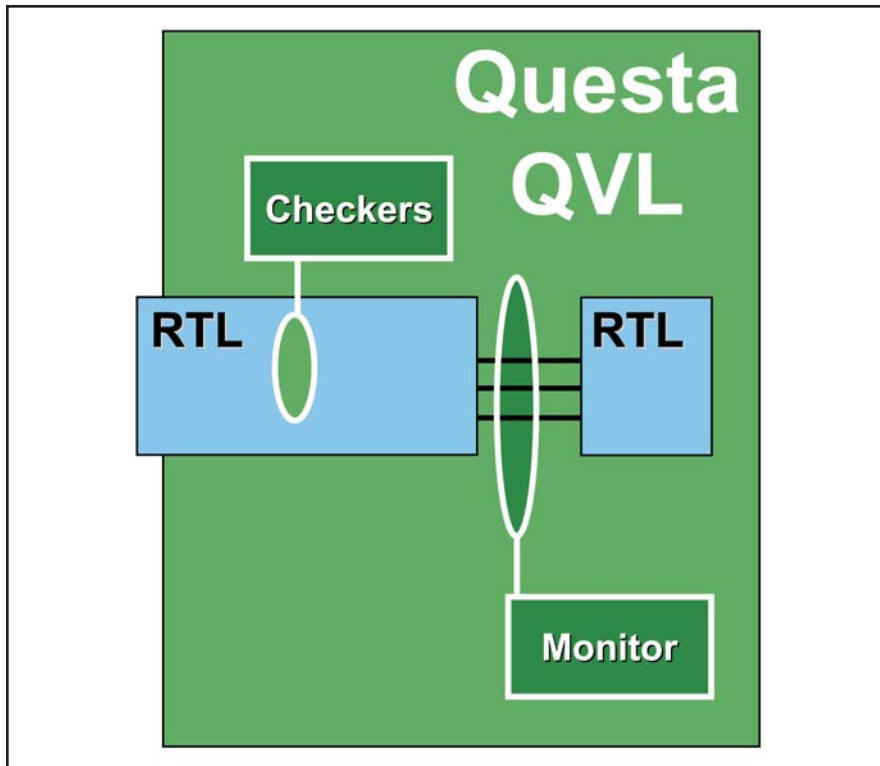


# Questa Assertion Checker and Monitor Verification Library (QVL)

Advanced Functional Verification

D A T A S H E E T



*As the only assertion library optimized for formal verification, the QVL finds bugs that other verification techniques can not.*

## Improving Design Quality

Today, many SoC designers realize the value of assertion-based verification (ABV) for ensuring a higher quality end-product. By instrumenting RTL designs and interfaces with assertions, ABV checks for the expected design intent and any unintended behavior, with violations reported to the designer at the instant they occur. Assertions act as watchdogs that stay with the design from the module/block level, through the integration of clusters into units, and on to the chip level.

The Questa® Verification Library (QVL) is a comprehensive SystemVerilog library of proven industry protocols and assertion checkers. Because QVL assertions are optimized for formal verification, designers can reuse the same assertion checking solution in simulation and formal verification—detecting bugs that other verification techniques can not.

QVL checkers and protocol monitors accelerate the construction of advanced verification environments, improve bug detection, and attain verification closure sooner for a better design in less time.

## Major product features:

- Complete SystemVerilog library solution for assertion-based verification (ABV) with checkers and protocol monitors
- Fast adoption and deployment of ABV with both simulation and formal verification
- With built-in structural coverage, integrates into any coverage driven methodology
- Finds hard bugs, ensures interface robustness, and verifies integration correctness
- Provides actionable metrics to improve verification coverage
- Integrates with Questa Multi-View Verification Components (MVC), Verification Management, and Unified Coverage Database (UCDB)
- Based on Mentor 0-In® CheckerWare technology
- Delivered with Questa SV and Questa AFV
- Extends Accellera's standard OVL with over 50 advanced and optimized assertion checkers
- Includes assertion monitors for popular standards such as: AMBA2 AHB, APB, APB3 and AMBA3 AXI, DDR SDRAM, DDR-II SDRAM, Gigabit Ethernet GMII, MII, XGMII, XAUI, XSBI, I2C, LPC, OCP, PCI, PCI-Express, SPI 4-2, SAS, SATA, USB1.1, USB2.0

## QVL Benefits

- Improves design quality and enables new verification techniques
- Easy to use, when instantiated in a design or testbench, checking starts immediately
- Pre-verified, optimized, and proven components avoid errors and eliminate high verification performance overhead
- Reusable in simulation and formal verification



*The Questa functional verification platform delivers the most comprehensive verification capabilities in the industry.*

## Accelerating Adoption of High Productivity Verification Methods

Combining the QVL with the Questa verification platform, the Open Verification Methodology (OVM), and standards like SystemVerilog, Mentor is clearly the leader in opening the doors to broader adoption of newer, higher-productivity verification flows. The QVL detects bugs at the source for faster turnaround times and accelerates closure with structural coverage.

## Questa Functional Verification Platform

The Questa functional verification platform combines high performance and high capacity with the most comprehensive verification capabilities in the industry. Assertion-Based Verification (ABV), assertion libraries (QVL), intelligent testbench automation (inFact), multi-view verification components (MVC), and coverage-driven verification (CDV) are supported natively by the Questa platform's high-performance assertion engine, constraint solver, and extensive functional coverage features, including verification management leveraging the Unified Coverage Database (UCDB). Verification of low power design functionality can be proven in an RTL environment using Power-Aware functional verification. This full set of advanced verification functionality is enabled by a flexible Open Verification Methodology that delivers unrivaled language and feature support in any design and verification flow.

### QVL Assertion Checkers include:

*qvl\_arbiter, qvl\_assert\_follower, qvl\_assert\_leader, qvl\_assert\_timer, qvl\_assert\_together, qvl\_back\_pressure, qvl\_bits\_off, qvl\_bits\_on, qvl\_bus\_driver, qvl\_bus\_id, qvl\_change\_timer, qvl\_channel\_data\_integrity, qvl\_constant, qvl\_content\_addressable\_memory, qvl\_coverage, qvl\_crc, qvl\_data\_loaded, qvl\_data\_used, qvl\_decoder, qvl\_decoder\_8b10b, qvl\_driven, qvl\_encoder, qvl\_encoder\_8b10b, qvl\_fifo, qvl\_gray\_code, qvl\_hamming\_distance, qvl\_known, qvl\_maximum, qvl\_memory\_access, qvl\_minimum, qvl\_multi\_clock\_fifo, qvl\_multi\_clock\_multi\_enq\_deq\_fifo, qvl\_multi\_clock\_multi\_port\_memory, qvl\_multi\_enq\_deq\_fifo, qvl\_multiplexor, qvl\_mutex, qvl\_outstanding\_id, qv\_parallel\_to\_serial, qvl\_req\_ack, qvl\_resource\_share, qvl\_same, qvl\_same\_bit, qvl\_same\_word, qvl\_scoreboard, qvl\_serial\_to\_parallel, qvl\_stack, qvl\_state\_transition, qvl\_three\_state, qvl\_timeout, qvl\_value, qvl\_value\_coverage, qvl\_xproduct\_bit\_coverage, qvl\_xproduct\_value\_coverage*

**Visit our web site at [www.mentor.com/qvl](http://www.mentor.com/qvl) for the latest product news.**

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