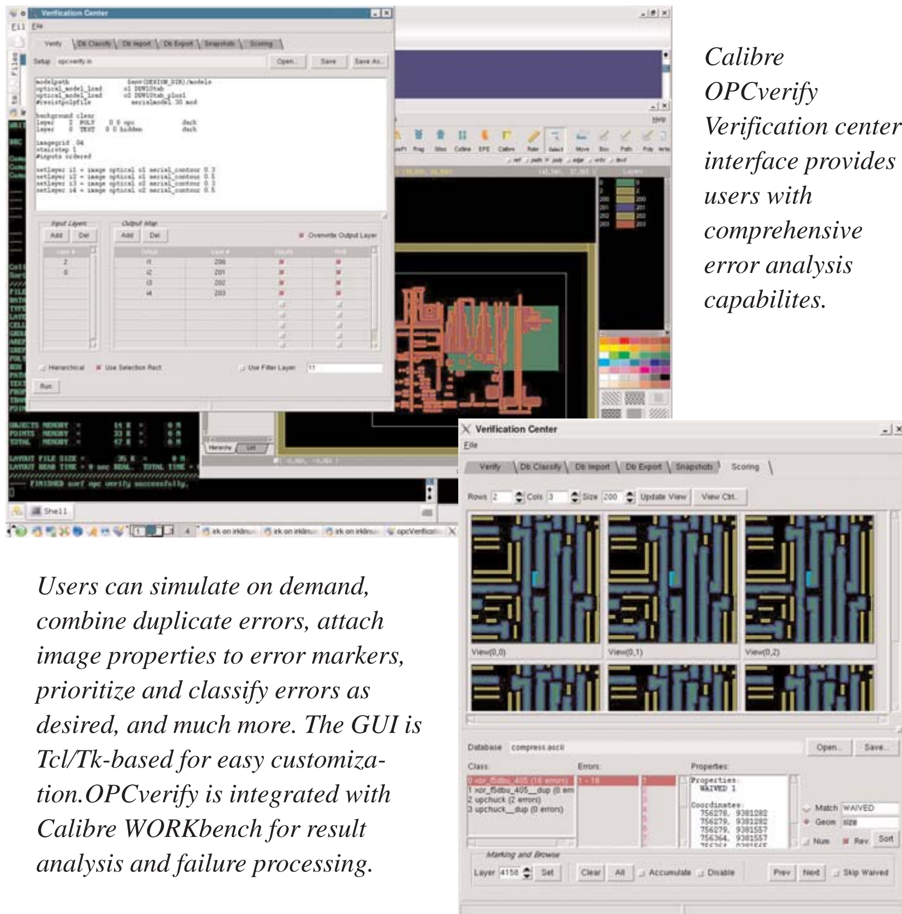
Calibre OPCverify

D A T A S H E E T



Calibre OPCverify Verification center interface provides users with comprehensive error analysis capabilites.

Users can simulate on demand, combine duplicate errors, attach image properties to error markers, prioritize and classify errors as desired, and much more. The GUI is Tcl/Tk-based for easy customization. OPCverify is integrated with Calibre WORKbench for result analysis and failure processing.

Calibre OPCverify: New grid-based simulation enables "virtual manufacturing" for 65 nanometer and below

Current low k1 photolithography processes are increasing the complexity of resolution enhancement technology (RET) applications in nanometer designs. This has resulted in higher silicon failure rates caused by mask rule constraints, fragmentation, modeling and metrology errors, and more. To reduce errors, a post-OPC verification step is needed to detect failures before a design is sent to the mask or wafer manufacturer. Calibre® OPCverify "overlays" a virtual grid on the design to measure every element and contour, not just edges, providing critical failure detection and full process window prediction.

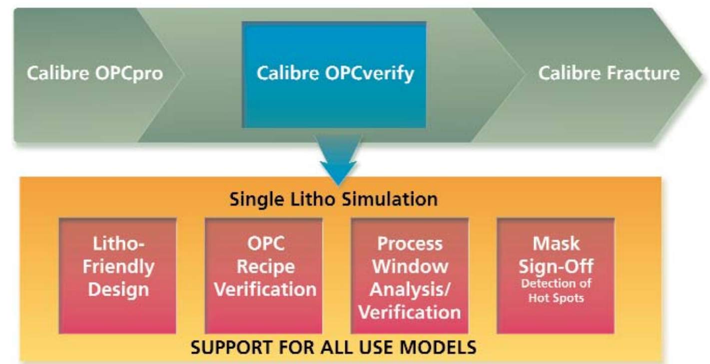
Results ouput can be customized and integrated to the user's flow. Calibre OPCverify enables a "virtual manufacturing" lithography simulation to determine pattern transfer accuracy.

Key Product Benefits

- **Grid-based OPC simulation** eliminates need for user defined simulation sites, making setup fast and easy.
- **Simulates how a design will manufacture through the process window**, allowing users vary RET recipes and determine best OPC score for manufacturing of design.
- **Provides accurate wafer contour simulation** for advanced process conditions, including immersion litho.
- **OPC usage models supported**, including OPC recipe verification, mask sign-off, litho-friendly design, VT5 and optical.
- **"Canned" and customizable** scripts for CD errors, spacing errors, bridging and pinching checks, and two-layer checks.
- **Results output can be customized** and integrated to the user's flow.
- **Supported by the Calibre platform** and hierarchical polygon processing engine.

Single, Accurate Modeling Foundation for all Lithography Simulation

Calibre OPCverify is the cornerstone technology that anchors the next generation of resolution enhancement technologies and design for manufacturing solutions. Calibre OPCverify uses the production proven accuracy of the Calibre OPC models to predict printed contours through process window conditions, including those of immersion lithography. All verification checks are enabled through the Verification Center user interface and done through user- specified Dose and Focus settings. Checks include pinching, bridging, extra printing features, non-printing features, CD variation (ACLV), CD errors and 2-layer enclosure checks.



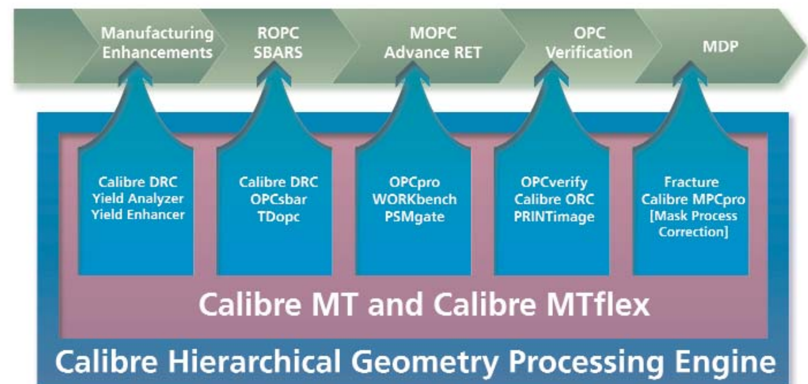
OPCverify simplifies lithography support and entails all required use models for verification technology.

Calibre offers a Complete Design-to-Silicon Platform

A powerful hierarchical engine is at the heart of the Calibre tool suite, which offers a complete IC and SoC design-to-manufacturing solution. Each tool is an excellent point tool on its own, but the combination of Calibre DRC, LVS and RVE with Calibre xRC, Calibre Calibre RET and Calibre MDP and design for manufacturing solutions (Calibre YieldAnalyzer and Calibre YieldEnhancer) simplifies and strengthens the design flow. In addition, Calibre MT and Calibre MTflex enhance performance and reduce turn-around times across the platform.

The Calibre RET tool suite for Optical and Process Correction (OPC), Calibre OPCverify, Phase Shift Mask (PSMgate), OPCsbar (scattering bars), TDopc (model-driven OPC), and Off-Axis Illumination (OAI) deliver silicon accuracy, fastest turn-around-time and excellent yield.

Calibre MDP allows for seamless continuation of the data manipulations required for RET techniques to the mask data format conversion in one batch run, keeping data hierarchically represented as long as possible.



Calibre offers a unified flow from GDSII/OASIS to mask, with one command language, hierarchy preservation, flow-cycle time optimization, common core hierarchical processing engine, and common customer support.

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