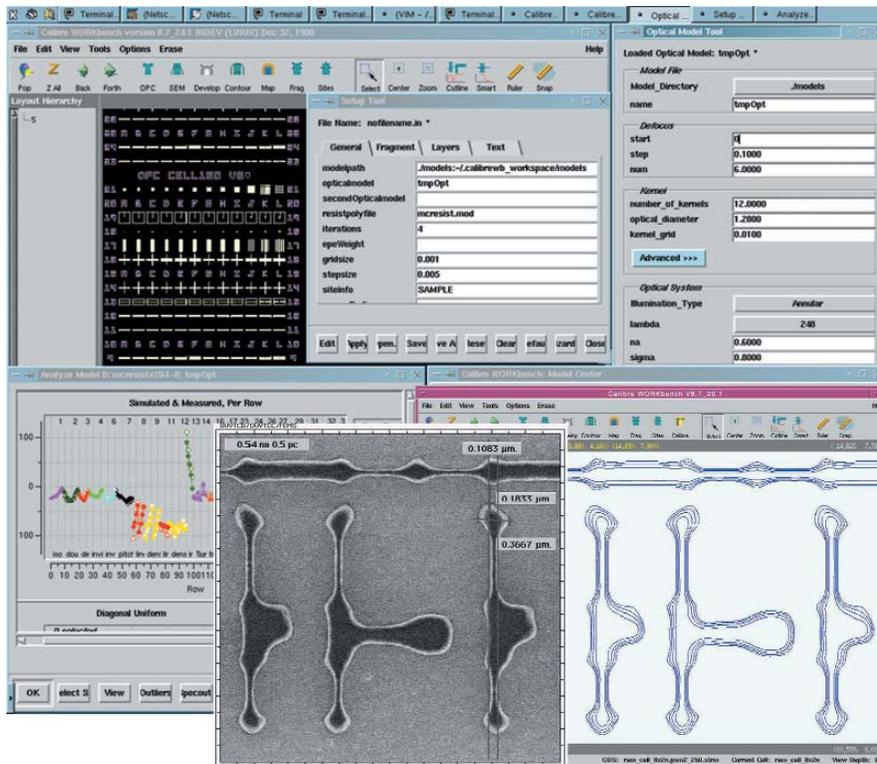


Calibre OPC and PSM



Calibre offers easy to use process modeling and tool setup, with production-worthy accuracy and enhanced turn-around-time. The Calibre WORKbench screen above shows some of the modeling and graphing tools. The highly accurate Calibre simulation (lower right) matches the SEM (Scanning Electron Micrograph) wafer image (lower left).

Calibre OPC and PSM: Enabling Silicon Accuracy, Speed and Yield from 180nm to 65nm and Beyond

The Calibre product line's subwavelength tools—such as Calibre OPCpro, Calibre ORC, Calibre PSMgate and Calibre OPCsbar—are the first complete design-to-silicon solution. By deeply integrating OPC (optical and process correction), PSM (phase-shift mask) and SB (scattering bar) technology with the industry's physical verification standard, Calibre DRC and Calibre LVS, the Calibre solution delivers silicon accuracy, fastest turn around time available, and excellent yield. The benefits will be realized with the largest designs and with the complexity of OPC and PSM correction layers to be reliably corrected and verified overnight.

Key Product Benefits

Accurate sub-wavelength silicon: Calibre's high-NA vector model, TCCcalc, and new process model, VT5, will ensure unsurpassed accuracy RET (reticle enhancement technique) solutions.

One run, one job, one deck: Since Calibre's sub-wavelength tool suite is fully integrated into Calibre's physical verification standard, the full backend process can be executed within a single job deck, from post-layout to OPC and fracture.

Decreased production costs: Calibre's "mask-friendly" OPC and PSM output minimizes mask costs and lowers overall write times.

- **Flexible OPC choices:** Calibre's flexibility enables just the right amount of OPC to be applied for each run by offering a choice between rule-based OPC, minimizing compute intensity, and/or model-based OPC, maximizing correction thoroughness, even with PSM.
- **High performance chips:** A complete PSM solution enables printing of fast, small gates and other structures while minimizing variances.

Fast, Verifiable Production

Calibre's integrated design-to-silicon products provide a production-worthy environment unique to the Calibre architecture, including industry leading verification and design-for-manufacturability correction. Consider the following strengths of the toolset (full-chip, batch production tools):

- Single software executable allows a single fast run to perform many post-layout processing steps, with no import/export database delays, while preserving the hierarchy. One run offers layer derivation, Boolean operations, SB, DRC, mixed rule/model-based OPC, PSM, phase-checking, ORC, LVS, mask data preparation (including fracturing), planarization fill and more.

- Unified Calibre Standard Verification and Rules Format (SVRF) command language environment encapsulates all post-layout OPC/PSM processing and verification in a single job deck. This simplifies tool setup and flow deployment.

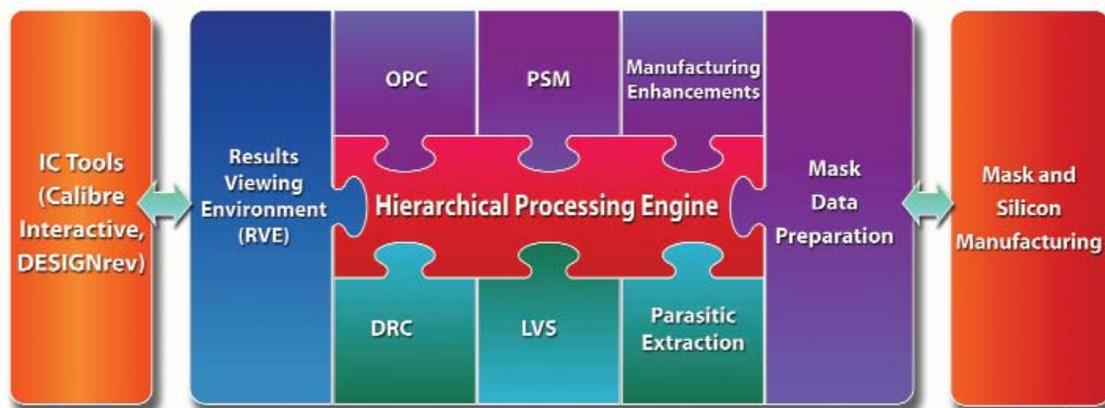
- The only available OPC/PSM/

Scatter Bars insertion software that is the same software as the defacto industry standard for deep submicron verification.

- One powerful IC database engine for all processing delivers consistent design integrity and minimal data expansion, while enabling faster turn-around-time advantage over competing tools. Fast and scalable in either multi-threaded or distributed platforms to take advantage of multiple CPUs to speed execution.

Calibre DRC (Design Rule Checking) has a much broader role than geometry checking in the demanding world of sub-wavelength manufacturability. The advanced Calibre IC database processing engine in Calibre DRC is used for many tasks in a single run. These tasks include rule-based OPC, planarization fill, antenna checks, multi-threaded or distributed parallel data processing, design-independent hierarchy handling and many other advanced post-layout tasks in Calibre's integrated verification and manufacturability environment.

Calibre ORC (Optical and Process Rule Checking) provides full-chip batch checking for IC manufacturing "printability" problems, called EPEs (Edge Placement Errors). Calibre ORC uses a calibrated optical and/or process model developed from the process characteristics. Calibre ORC predicts the silicon location 1D and 2D structures of interest in the design (e.g. line-ends, corners, or user-defined structures). If the EPE for that type of structure is greater than a user-set tolerance, the software outputs an "error box" over the edge in a new GDSII output layer, as well as report outputs, including statistics. In addition to predict EPE, Calibre OPC has a rich set of functionality that can predict optical and process characteristics of the layout in combination of the geometrical characteristics. Integration with popular layout editors is provided through Calibre RVE (results viewing environment), enabling easy debug and viewing of results. Calibre ORC's capabilities are also available in the Calibre OPCpro license.



The Calibre Design-to-Silicon product line integrates Resolution Enhancement Technologies (OPC, PSM, SB) with the industry standard for deep submicron physical verification. For production engineers, Calibre offers a unique system of integrated full-chip batch tools for unsurpassed turn around time (TAT).

Calibre TDopc (Table-Driven OPC) is a product with two commands: OPCBIAS and OPCLINEEND. The first command makes it easy to do fast rule-based OPC for line widths based on a simple table of values. The second command makes it easy to apply line-end treatments, such as hammerheads, based on a simple table of values. Calibre TDopc's capabilities are also available in the Calibre OPCpro license.

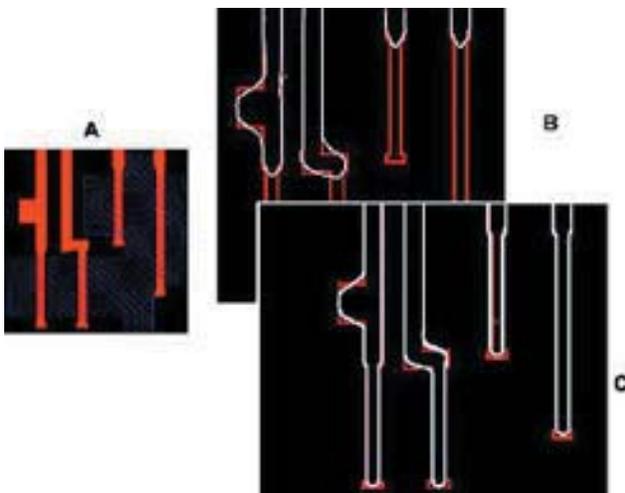
Calibre PRINTimage (Simulated Silicon Print Image) produces a full-chip, batch output of simulated silicon shapes, and enables simplified DRC checks on these shapes, or "silicon DRC". The simulation is based on the optical model and process model developed from the process characteristics. The simulator handles PSM effects, including attenuated PSM side-lobe detection and strong PSM phase imbalances. The simulated silicon shapes are output in a new GDSII output layer.

Calibre OPCpro (Optical and Process Correction for Batch Production) provides full-chip batch correction of the input layout in order to increase yield and process latitude. The software makes changes to the layout to compensate for lithography distortions inherent in the deep sub-micron manufacturing process. Any mix of rule and/or simulation-based correction can be used. The simulation is based on the optical model and process model developed from the process characteristics. Calibre OPCpro includes the functionality of Calibre ORC; it is fully capable of correcting phase-shifted layouts, attenuated or alternating PSM for gates being the two most common types supported.

Calibre PSMgate (Phase Shift Mask Assignment for Gates) provides full-chip, batch phase assignment to increase yield and chip speed for sub-wavelength lithography using existing manufacturing equipment. The

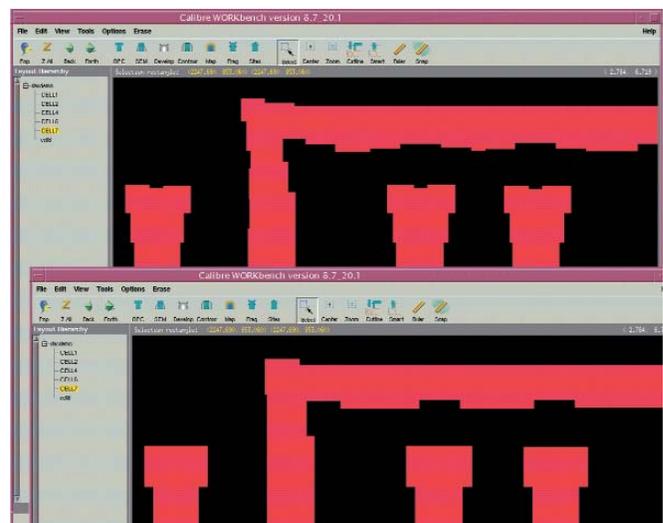
software, along with related Calibre commands, makes changes to the layout to enable significantly smaller gate features than the wavelength of the light used in manufacturing. Calibre OPCpro's model-based OPC algorithms are "phase-aware," so phase distortions typically found near phase transitions and line ends can be corrected.

- Many types of PSM techniques can be both assigned and verified, such as one-/two-exposure and two-/three-/four-phase methods. Although primarily used for one-half to one-third wavelength sized gates today, the assignment algorithm can be applied to other selected layers/structures as well.
- Calibre is also used today for full-layer PSM, including the critical interconnect around gates.
- Calibre's powerful layout processing engine enables layer derivations, Boolean operations, and phase-

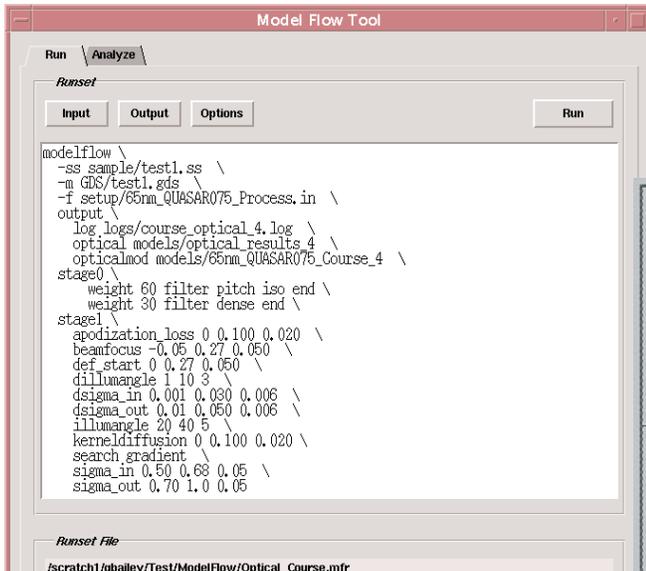


Results of OPC on PSM:

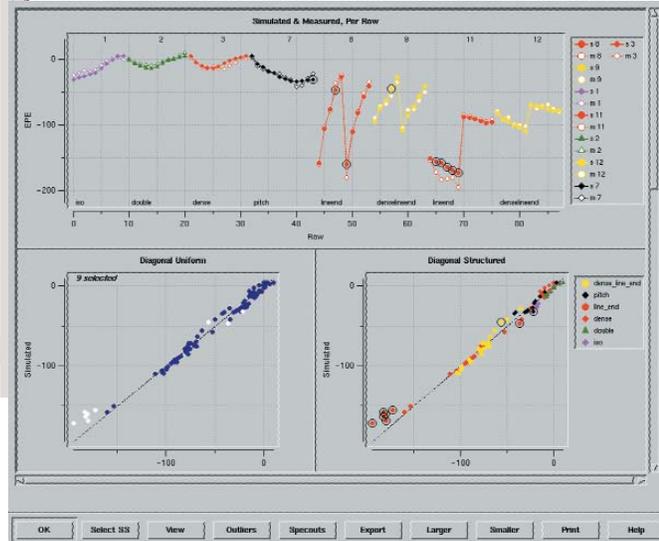
- A** = original layout with layer gates
- B** = PRINTimage output of original, uncorrected layout
- C** = PRINTimage output after PSM and phase-aware multi-layer OPC, including differential MEF



Calibre OPCpro offers very flexible options for OPC from moderate to more aggressive correction.



Calibre WORKbench Model Flow Tool automates the full optical and process model calibration routines along with results analysis.



Calibre WORKbench Model Center has easy yet powerful graphing capabilities to visualize and fine tune model accuracy.

conflict checking essential to a strong or attenuated complete PSM flow. Examples include shape-based checking, long-range “colorability” and side-lobe detection and correction.

Calibre OPCsbar Scattering Bars (SBs) are sub-resolution, phase or chrome bar-like features placed near the edges of patterns on the reticle. Anti-scattering bars (ASBs) are simply the inverse of SBs and are embedded into the pattern. SBs and ASBs alter the slope of the aerial images of isolated and semi-isolated lines to better match those of densely-nested lines. By doing so, scattering bars help maintain adequate depth of focus across pitch to help in reducing aberration effects and CD dispersion. Calibre can add, simulate and verify SBs, while retaining hierarchy. Implement SBs with the easy-to-use Calibre OPCsbar product, or create them with your own Calibre

script. OPCsbar has a sophisticated, priority-based “cleanup” option to help decide which SBs to keep when they overlap.

Calibre’s Solution for Accurate Tool Setup

Calibre WORKbench is a stand-alone application for use primarily by lithographers. It is an easy-to-use environment for creating accurate process models and tested production-ready tool setup files. These approved models and setup files are then handed off to production users to drive turnkey IC layout RET processing.

Calibre WORKbench software can create test patterns for silicon measurement, as well as run test jobs in order to test and visualize the outputs of the models and setup files. It contains a fast, high-capacity layout viewer with easy-to-use interactive lithography simulation and visualization. It

supports GDSII and fracture format viewing.

Calibre WORKbench can also be used for advanced cell library design, integrated tightly with popular layout editors. For larger jobs, the Calibre full-chip, batch products are used. Features and benefits of Calibre WORKbench include:

- ModelCenter module makes it easy to create best-fitting process models from test pattern data.
- Customized or standard illumination source types (tophat, annular, quadruple, QUASAR, dipole, custom...).
- Thin film stack generation for high-NA vector modeling, TCCcalc.
- Very fast layout viewer, integrated with lithography simulators and editors: GDSII and fracture formats. Advanced process models (photore-sist, etch,...) with default or user defined convolution shapes and

image parameters enabled through VT5.

- Simulated views of layout include: optical-intensity map, printed image on the wafer, fragmentation sites, 2D cross-section intensity maps, multi-level print-image contours.
- Integrated execution of the batch tools on small, selected regions for testing.
- Automated model calibration through Calibre WORKbench Model Flow Tool.

Calibre LITHOview is a subset of Calibre WORKbench. It offers the same capabilities as WORKbench, except for model creation and test pattern generation. This tool is targeted for users to confirm layout or OPC model results without the need of model generation.

Calibre Hierarchy and Design Independence

Calibre is one of the most successful products in EDA history. Its rapid growth is primarily a result of its powerful hierarchical database engine, which was designed exclusively for the deep submicron era. Advanced IC processing heuristics such as Hierarchical Injection™, Selective Promotion™ and Bin Injection™ enable unique IC processing speed and capacity:

- Design independent setup: create one job deck per process, not per design.
- Design independent performance: one job deck runs fast “out of the box” on many design styles and for system-on-chip designs that contain many different styles (RAM, logic...).

- Minimal data expansion, even with full-chip OPC modifications.

Preserves hierarchy far better than any other tool. Cell count explosion in competing tools can be 50X-100X.

- Platform adaptable: one job deck for multi-threaded (MT) Unix environments or for distributed (MTflex™) processing in Linux clusters.

Mask-Friendly: Lowers Cost and Turn-Around-Time (TAT)

As the cost of subwavelength reticle sets grows ever larger and as mask TAT and inspection problems become more and more challenging, it is vital for OPC/PSM tools to ease the downstream tasks as much as possible. For example, Calibre’s OPC model-based algorithms and default settings have been tuned to be mask-friendly in collaboration with mask-industry partners:

- Default OPC shape generation has been tuned for mask-writing speed, and for zero false errors at mask-inspection time.
- Minimal data expansion avoids downstream mask-processing problems.
- Layouts modified for PSM are checked for troublesome small jogs with MRC (mask rule checks) and fixed.
- Calibre can generate write-ready fracture formats.

Flexible Correction Strategies

“Just enough OPC” is the best policy for successful correction. The Calibre manufacturability tool suite allows easy and flexible flows combining these capabilities:

- Rule-based-OPC uses DRC licenses you may already own, or use Calibre TDopc with ORC for model-based checking.
 - Automatic model-based OPC can recognize rule-based OPC corrections with no setup required, and take the right action for incremental correction.
 - Model-based OPC algorithms are “phase-aware” to handle layout structures that can be attenuated or strong PSM, or single or multi-exposure.
 - ORC and print-image verification tools check for unintended side-effects of attenuated PSM region interactions, sometimes called “dimples” or “side-lobes.”
 - Different correction or verification policies can be applied by structure type (line-ends, corners, etc.), by layer, or by block.
-

Summary

The Calibre Design-to-Silicon solution is unique in the marketplace. It is the only tool suite that is production-worthy and truly integrates industry leading verification with a full suite of full-chip OPC, PSM and SB tools. This provides:

- Unsurpassed turn-around-time.
- Design independent tool setup and consistently fast run-times with highly scalable multi-threading and distributed performance.
- Verifiable data integrity.
- Mask-friendly output and low data expansion.
- Extends the practical life of manufacturing equipment.
- High-NA Vector and extensive process modeling capability for leading edge RETs.
- Robust subwavelength process windows for yield and profitability.

For more information or for articles and technical papers, please visit the Mentor Graphics website at www.mentor.com/dsm

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