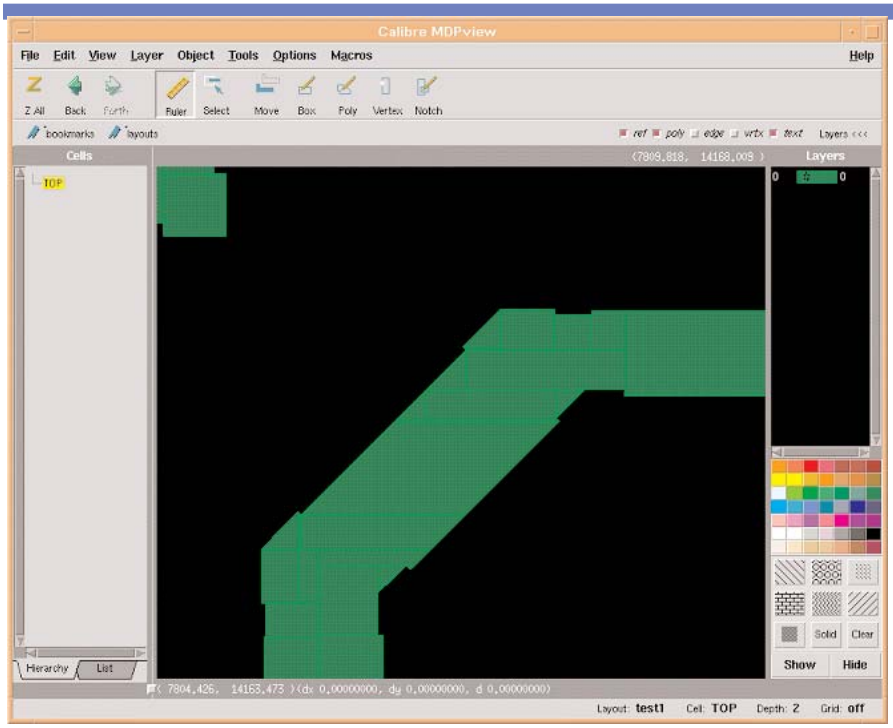
Calibre FRACTUREt

Toshiba VSB11 Formatted Mask Data Export

Manufacturability

D A T A S H E E T



Calibre FRACTUREt enables direct data export from the Calibre database into Toshiba's VSB11 format. The illustration shows a section of the VSB11 formatted file in the viewing tool.

Mask Data Preparation for Toshiba VSB11 Format

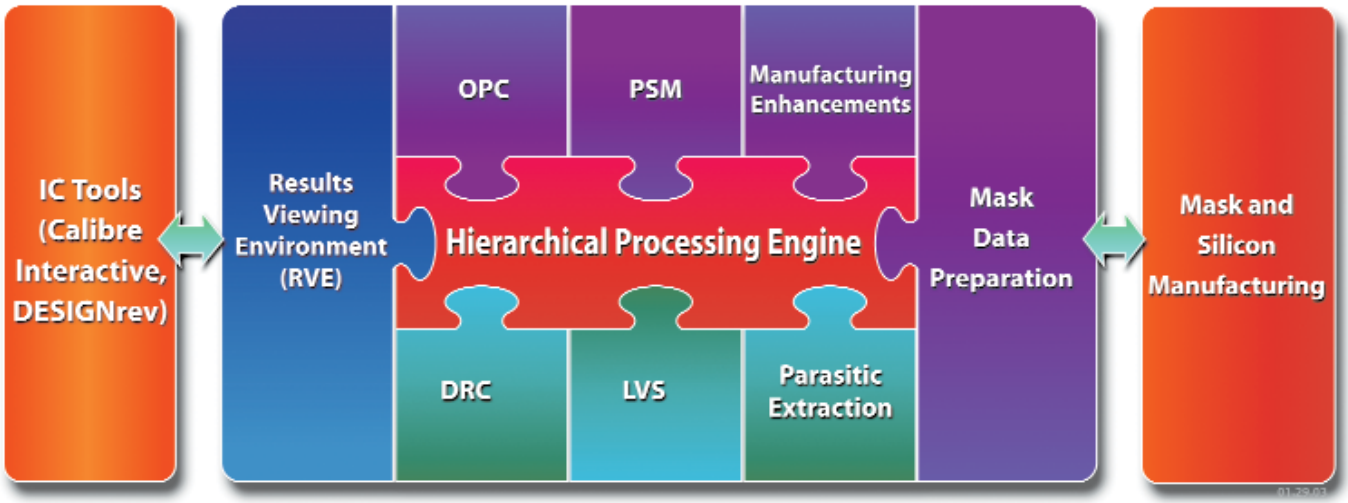
Calibre® FRACTUREt™ expands the Calibre product line from physical verification (DRC/LVS) and resolution enhancement techniques (RET) into mask data preparation (MDP). After conducting complex optical proximity corrections like rules-based or model-based OPC, or general sizing and Boolean operations, data can now be exported directly into the Toshiba mask writing format (VSB11) without changing tools or creating large intermediate files. Data processing is conducted utilizing Calibre's powerful hierarchical engine. This enables fast processing speeds in addition to an optimization of the output for most efficient mask writing. Small figures are efficiently suppressed and the shot count is minimized. File size is kept to a minimum by utilizing hierarchy and an optimized fracture algorithm.

Calibre FRACTUREt is complemented by a dedicated verification command, MDPverify, which allows for an independent verification of the fractured results against the original GDS file or a previous version of the VSB11 output.

Key product benefits:

- Build on hierarchical geometry processing inside the Calibre database for Boolean and sizing operations
- Hierarchical fracturing for fast processing speed
- 32/64 bit on HP, Sun and Linux platforms
- Multi-threading with excellent scaling performance
- Dynamic memory allocation
- Optimized fracture algorithms enable minimized shot count
- Optimized for mask writer performance enabling high mask writer throughput
- Efficient suppression of small figures
- Easy to integrate in an OPC and verification flow
- Combined with a verification command for comparison to GDS and mask writer formats
- No intermediate files

Mentor Graphics®



The Calibre tool suite offers a complete design-to-silicon solution to ensure a confident design for manufacturing.

Calibre Offers a Complete Design-to-Silicon Solution

A powerful hierarchical engine is at the heart of the Calibre tool suite, which offers a complete IC and SoC design-to-manufacturing solution. Each tool is an excellent point tool on its own, but the combination of Calibre DRC™, Calibre LVS™ and Calibre RVE™ (results viewing environment) with Calibre xRC™, Calibre RET and Calibre MDP, simplifies and strengthens the design flow.

Calibre xRC parasitic extraction tool accurately models the parasitic effects of passive interconnects that can cause design failure in deep submicron IC designs. Automated interfacing of Calibre LVS to Calibre xRC provides simplicity (one rule file, one invocation) and automated back annotation for accurate parasitic extraction results, and ensures accurate and intentional device extraction with parameter calculation and parasitic device extraction for accurate simulation.

Calibre Interactive™ complements the Calibre physical verification tool suite by enabling designers to perform verification from within Cadence Virtuoso® and Mentor Graphics IC Station™ and Calibre DESIGNrev™. Together with Calibre RVE, Calibre Interactive provides a seamless, push-button interface, enabling designers to use a single platform for cell/block and full-chip physical verification.

The Calibre RET tool suite for Optical and Process Correction (OPC), Phase Shift Mask (PSM), Scatter Bars (SB) and Off-Axis Illumination (OAI) deliver silicon accuracy, fastest turn-around-time and excellent yield.

Calibre MDP allows for seamless continuation of the data manipulations required for RET techniques to the mask data format conversion in one batch run, keeping data hierarchically represented as long as possible.

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