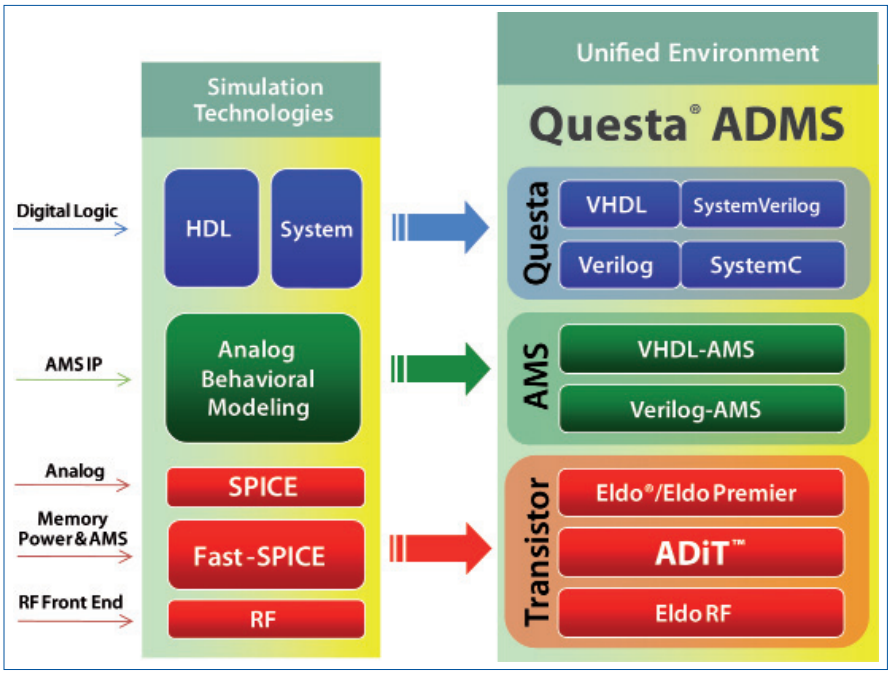
AMS-Targeted Fast-SPICE Simulator
ADiT

Analog/Mixed-Signal Verification

D A T A S H E E T



ADiT is a Fast-SPICE simulator built specifically for analog and mixed-signal applications and is part of the Mentor Graphics AMS simulation family.

Highly Accurate Mixed Signal Analog Verification

The Mentor Graphics ADiT™ (Analog Digital Turbo Simulator) is an advanced Fast-SPICE simulation tool targeting analog and mixed-signal (AMS) transistor-level applications. It features a mixed-signal aware partitioning algorithm that allows fast and accurate simulation of circuits with non-ideal power supplies. It also embeds built-in SPICE with chargeconserving analytical and table-based device modeling to deliver accurate, reliable results 10 to 100 times faster than traditional SPICE simulation. With a compact data structure, smart partitioning, and a look-up table, ADiT can handle chip-level simulation with more than 10 million devices.

ADiT supports Eldo® Classic and Eldo Premier, HSPICE, and Spectre netlist formats. It is also integrated into the Questa® ADMS™ mixed-signal simulation solution, supporting full-chip SoC verification.

Non-Ideal Power Design Simulation

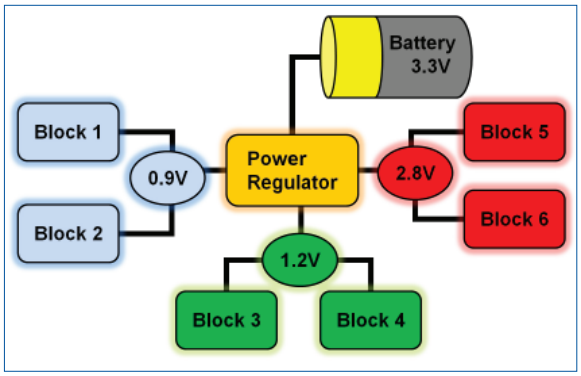
Conventional Fast-SPICE simulators use DC-connected partitioning. In other words, all nodes belonging to the same DC path are grouped together. With ideal VDD and VSS signals, the DC-connected partitions can be isolated, and

FEATURES AND BENEFITS:

- 10–100X speed improvement in transistor-level verification of complex AMS circuits
- Three percent accuracy of results by integrating SPICE and Fast-SPICE engines
- Over 10M device capacity
- Seamless mixed-signal SoC verification through integration into Questa ADMS simulator
- Smart partitioning algorithm
- Default table-look up modeling with an equation-based device modeling option
- Charge-conserving device models
- Hierarchical parsing
- Non-ideal power simulation
- Support of most device models
- Reliability (aging) analysis
- Post-layout back annotated and RC reduction
- Co-simulation with third-party Verilog simulators via ADiT-VPI
- Hi-Z and leakage current detection
- Monte Carlo analysis
- Save/restart with ADiT
- Netlist support: Eldo Classic, Eldo Premier, HSPICE, Spectre
- Verilog-A/AMS support
- Output formats: JWDB (.wdb), FSDB (.fsdb), ADiT (.TR0/.TB0)
- Platform support: RedHat Enterprise Linux (32, 64 bit)

Mentor Graphics®

hence they can be solved individually. However, in today's battery-powered designs, the VDD and VSS signals are usually regulated with an internal power supply, and they are no longer ideal. This is why typical Fast-SPICE simulators cannot handle derived rail designs well. ADiT's proprietary circuit partition scheme and derived rail algorithm allows fast and accurate simulation of non-ideal power designs.



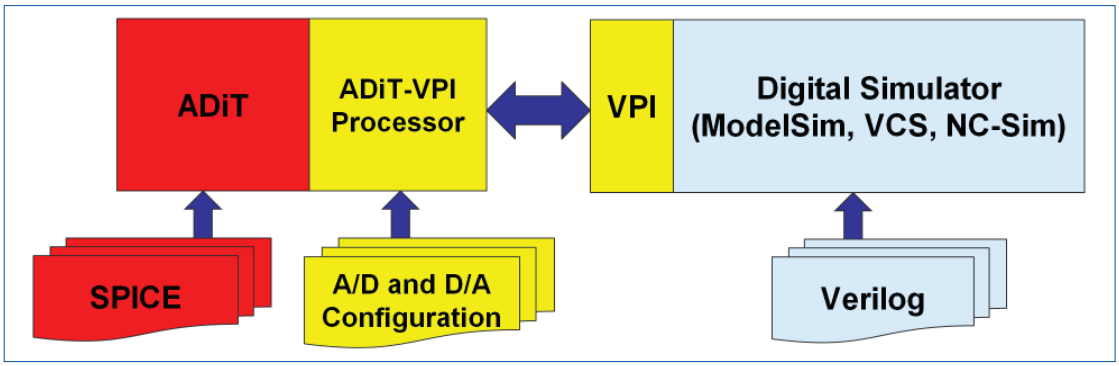
Derived rail algorithm handles non-ideal power designs with speed and accuracy.

Integration with Questa ADMS

The integration of ADiT into Questa ADMS provides the optimal platform for mixed-signal, full-chip SoC verification. ADiT provides a stable and accurate Fast-SPICE engine for analog circuit simulation, while Questa ADMS offers fast digital Verilog/VHDL simulation. The Questa ADMS platform ensures accurate and efficient communication between ADiT and Questa. In addition, the support of VHDL-AMS and Verilog-AMS behavioral languages allows higher levels of circuit abstraction, which enables earlier design verification and faster full-chip simulation.

Co-Simulation with Other Digital Simulators

The optional ADiT-VPI package extends the capabilities of ADiT to deliver mixed-signal, full-chip co-simulation and integration with non-Questa digital simulators; such as VCS and NC-SIM. Using ADiT-VPI, designers can take full advantage of their existing HDL verification environment while running faster SPICE/analog dynamic simulations.



ADiT-VPI allows mixed-signal co-simulation with ADiT and third-party HDL simulators.

For the latest product information, call us or visit: www.mentor.com

©2012 Mentor Graphics Corporation, all rights reserved. This document contains information that is proprietary to Mentor Graphics Corporation and may be duplicated in whole or in part by the original recipient for internal business purposes only, provided that this entire notice appears in all copies. In accepting this document, the recipient agrees to make every reasonable effort to prevent unauthorized use of this information. All trademarks mentioned in this document are the trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
Room 1001, 10F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886.2.87252000
Fax: 886.2.27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

MGC 04-12 1030370-w