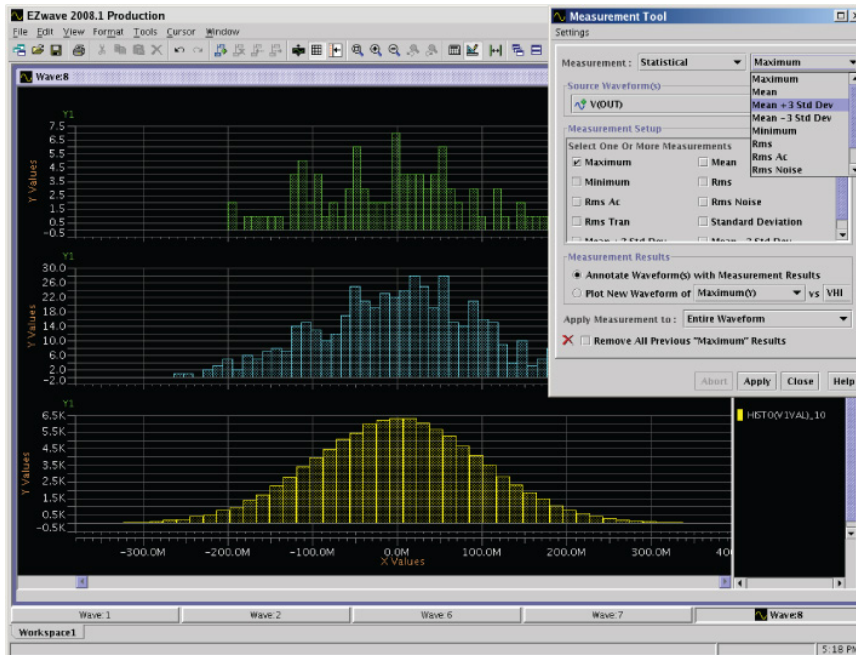


Eldo Classic

Integrated Circuit Simulation

Analog/Mixed-Signal Verification

D A T A S H E E T



Sophisticated statistical and sensitivity analyses will help you maximize the yield of your design, even when using high variability processes. With safe operating area checks, Monte Carlo, transient noise, DC mismatch, and aging analysis, Eldo Classic is a feature-rich simulator with sign-off level accuracy, armed for the most demanding IC designs.

HIGH-PERFORMANCE INTEGRATED CIRCUIT SIMULATION

With the capacity to handle the largest designs at the finest level of detail and the accuracy to detect design errors early in the development cycle, Eldo™ Classic simulator is the right tool for DSM design in the new millennium. Its ease-of-use and improved convergence allow a designer to focus on analyzing results, not on driving the tool.

Eldo Classic is the simulator of choice for IC silicon vendors and fabless design centers because of its speed, accuracy, and capacity.

Speed — When compared to other commercial or internal SPICE simulators, engineers who use Eldo Classic routinely report a 3x to 10x speed-up ratio without compromising accuracy, when compared to silicon.

Key Features

- Matrix solvers that efficiently handle large circuits.
- Scalable multi-threading technology.
- Optimized for library characterization tasks.
- EZwave™ graphical post-processor enables waveform analysis and post-processing.
- Eldo Classic supports all standard device models.
- Includes a large variety of macro-models.

Key Benefits

- Scalable multi-threading performance provides 3x to 10x gain in simulation speed and accelerates verification cycle.
- Sign-off level accuracy allows verification of complex analog IP and mixed-signal SoC without compromise.
- Tight integrations to IC design frameworks from Mentor Graphics and Cadence Design Systems maximize productivity.
- Eldo-certified electrical models are available from major foundries such as TSMC, UMC, Chartered, and STMicroelectronics.

Accuracy — For 25 years, Eldo Classic has been used to verify and successfully fabricate thousands of ICs, from the most modest ones to huge mixed-signal SoCs, in all domains of applications, from defense to communications to automotive, and on all continents. For designers, Eldo Classic is the absolute, golden, sign-off reference.

Capacity — Designers worldwide use Eldo Classic on designs ranging from a single cell to systems of 300,000 transistors or more. Compared to most SPICE tools, Eldo Classic exhibits a much more linear growth of CPU time with the size of the circuit. The raw maximum capacity of Eldo Classic is limited only by the amount of available RAM.

FOUNDRY SUPPORT

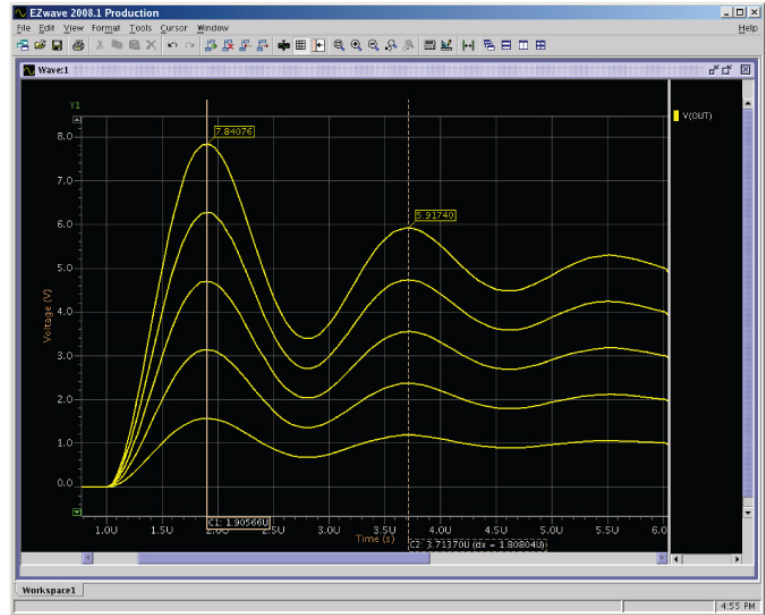
Eldo Classic is supported by all major foundries, including TSMC, UMC, Chartered, and STMicroelectronics, who deliver certified Eldo Classic electrical models to their customers. Eldo Classic can read and simulate netlist and libraries formatted for other simulators without modifications.

POST-LAYOUT SIMULATION

Eldo Classic includes matrix solvers that efficiently handle large circuits. Dedicated mixed linear/direct algorithms provide spectacular speed-up. Huge parasitic networks originating from layout extraction can be included and accurately simulated. Eldo Classic can use either flat or hierarchical DSPF information, with options for advanced filtering and selective inclusion of nodes or instances.

MULTI-THREADING

Eldo Classic contains scalable multi-threading technology to fully exploit modern multiprocessor computers. Depending on the circuit profile, the cost in analog simulation is either the complex device evaluations or the matrix resolution (or both). In Eldo Classic, the entire



resolution is multi-threaded, both the matrix solving and the device evaluations. Running on two CPUs usually provides a 1.5x speed-up. Running on four CPUs usually speeds up the simulation by 2x to 3x. For long simulation runs, such as PLLs, this can save days of waiting time.

MULTIPLE RUN SIMULATIONS

The cost of analog simulation is caused by the many corners and operating conditions that must be verified. Process, voltage, and temperature (PVT) verification before tape-out is vital for genuine analog IP verification because the variability of the processes has increased dramatically.

Eldo Classic offers a unique multiple-run mechanism, where such PVT simulations are transparently distributed in parallel onto the CPUs of a single machine or on the available network of machines. Multiple-run distribution also applies to data-sweep, worst-case, and Monte Carlo simulations. The mechanism is fully compatible with load-balancing tools such as LSF or Sun Grid and with proprietary dispatching tools. Because the simulations run in parallel, the net productivity gain

scales linearly with the number of CPUs or machines available.

The associated licensing scheme allows you to use inexpensive CPU hardware to run tasks that are 100% parallel. One run takes one license; two, three, or four runs take two licenses; and any four additional runs only take one additional license.

LIBRARY CELL CHARACTERIZATION

Library characterization can be a time-consuming task. Sensitivity to operating conditions, such as power supply and temperature as well as the slopes of the signals, has increased exponentially with each new technology node, calling for ever more simulations. The complexity of the device models such as BSIM4 or PSP and the short transition times of the signals require tight accuracy settings.

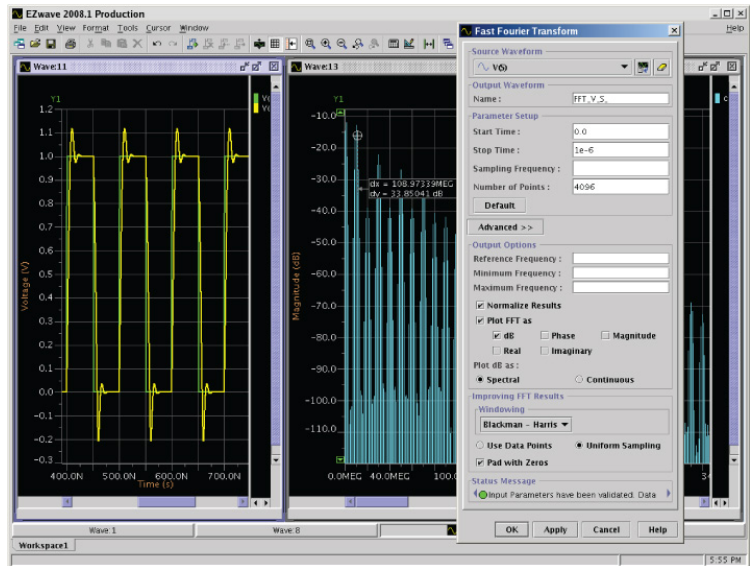
Most companies involved in cell characterization at 45 nm or less also include detailed RCC post-layout information in these simulations. Many of them also run additional statistical simulations to feed SSTA tools. All these factors extend global characterization times.

Eldo Classic is optimized for these library characterization tasks. It includes options that eliminate unnecessary overhead tasks associated with short simulations runs. Flexible commands are available to output measurement data in tabular form for easy post-processing.

Eldo Classic interfaces easily with third-party cell characterization tools. It features an interactive mode that can further speed up the process by eliminating system process launching time.

OPTIMIZATION

Eldo Classic includes a built-in multi-target multi-parameter optimizer that helps designers fine tune a design for optimal performance across multiple operating



conditions and process corners. The algorithms include classical simple bisection or secant techniques, but also much more sophisticated ones targeted at the efficient resolution of problems where the cost of evaluation is high: for example, optimizing the phase noise out of a VCO. The Mentor Graphics ICanalyst™ product offers a GUI for driving the optimization process.

VERILOG-A SUPPORT

The Eldo Verilog-A option complements Eldo Classic with a Verilog-A compiler that is compatible with the Verilog-AMS compiler in Mentor Graphics Questa® ADMS. Compiling and including Verilog-A modules in a netlist is easy and often allows significant speed up for system-level simulations or architectural exploration tasks. Verilog-A also can be used to extend core device models, such as BSIM4 or PSP, with additional custom parasitic effects for RF, high-voltage, or other specialized applications.

WAVEFORM ANALYSIS WITH EZWAVE

The EZwave™ graphical post-processor enables waveform analysis and post-processing. The native waveform format of EZwave, called “wdb” is extremely efficient for manipulating huge databases. EZwave can

load gigabytes of data in seconds. EZwave can also load most popular waveform formats. And it operates on both analog and digital signals.

DESIGN FRAMEWORK INTEGRATION

Eldo Classic is fully integrated both in the Mentor Graphics' IC flow and in the Cadence® environment. All functions such as netlisting, analysis, and options setup, cross-probing, and back-annotation are fully supported.

This includes advanced modules for corner-case or Monte Carlo analysis, optimizer support, and scripting, making it ideal if you don't want to edit any netlist. In the Cadence context, sophisticated utilities create the Eldo Classic views and libraries, or you can make direct use of existing libraries.

DEVICE MODELS

Eldo Classic supports all standard device models, including BSIM3, BSIM4, PSP, HiSIM, HiSIM/HV, EKV, HICUM, VBIC, MEXTRAM, BSIMSOI models, TFT models etc., covering all silicon technologies.

Mentor Graphics' device modeling experts participate in the Compact Modeling Council (CMC) and contribute to the support and continuous improvements of the state-of-the-art complex device models that are needed for technology nodes at 45 nm, 32 nm, and below.

Mentor strictly respects and accurately implements community-approved standards while at the same time aggressively optimizing performance. As a result, sophisticated device models such as PSP run significantly faster in Eldo than in any other competitive simulator.

Eldo usually supports the latest releases of the standard models and often include "pre-versions" when a model has not been officially released yet at the time of the Eldo release. A dedicated C-language API is available at no charge for easy and efficient implementation of proprietary models.

The API is the same one Eldo Classic uses for standard models, so the run-time performance of a proprietary model is not compromised.

MACRO MODELING

Eldo Classic includes a large variety of macro-models, i.e., components that cannot be described with elementary devices. These built-in models can be freely mixed with device models in a system description.

Built-in models include functional models (opamp, comparators, etc.), S parameters in Touchstone format, S and Z-domain filters, lossy dispersive transmission line models, and microstrip models.

Eldo Classic also supports the latest standard IBIS buffer models, including package models. All models can be encrypted for IP protection before final delivery.

AGING AND RELIABILITY MODELING

Eldo Classic includes a dedicated flow for the accurate prediction of performance degradation of ICs subject to hot carrier injection (HCI) and negative bias temperature instability (NBTI) effects. These undesirable physical phenomenon tend to degrade the performance of integrated circuits as time passes.

Below 130 nm, this cannot be neglected. The internal structure of transistors is gradually modified (damaged) and the electrical behavior eventually drifts. The deviation may cause the IC to fail to meet some aspect of its specification. Even worse, the deviation may be such that the IC suddenly ceases to function entirely.

The accurate modeling of wearing stress effects such as HCI or NBTI is under constant investigation. Thus, it is important to have the possibility to define arbitrary models. Using the "black-box" models provided in some canned solutions is simply unacceptable.

Companies concerned with accurate modeling of these issues are also concerned with confidentiality of their models. Eldo Classic addresses these concerns.

Models are written in C, compiled as binary dynamic libraries, and securely encrypted for additional protection against unauthorized use. This allows licensed partners, customers, and subcontractors to simulate reliability issues without revealing the details of the models.

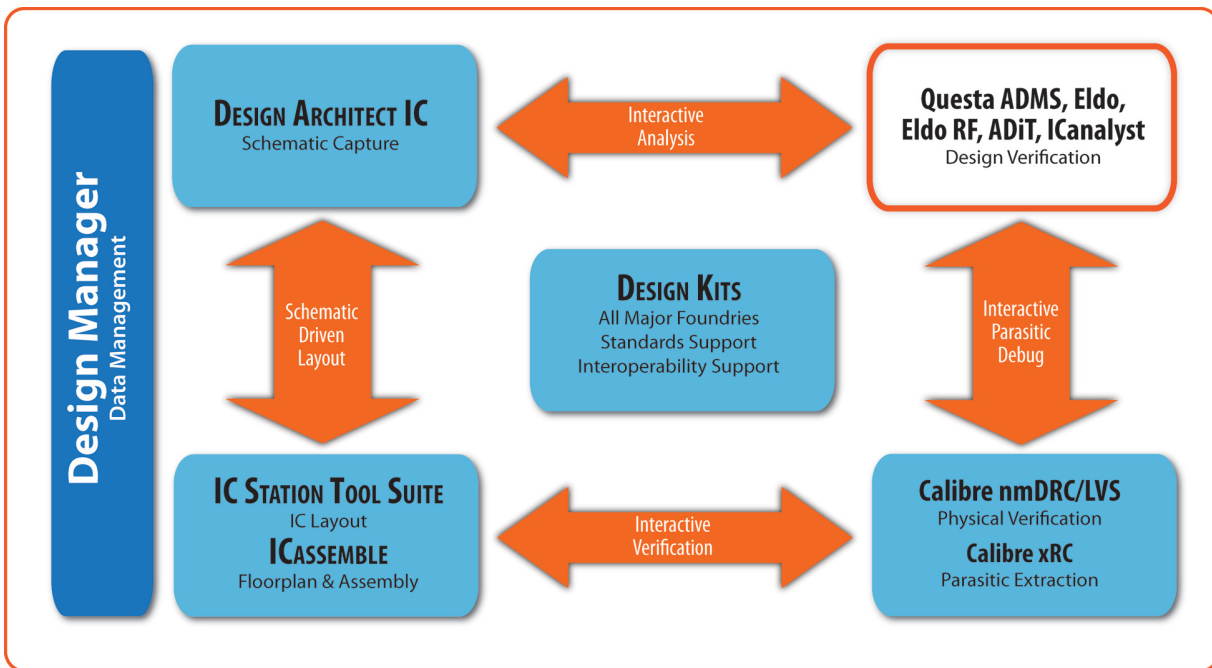
The Eldo Classic reliability solution, called User Defined Reliability Modeling (UDRM) extends Eldo transparently. There is no new environment to learn and only a minimal set of new commands, thus the learning curve is minimal. UDRM allows displaying overlapped fresh and “aged” waveforms, after any ar-

bitrary operation time, be it in seconds, weeks, months, or years.

The stress information can be saved and reloaded into another simulation, for example, a small-signal or noise analysis. Sorted degradation tables provide information about which devices are the most sensitive to aging. Source code template models that can be easily extended if necessary are provided, for both HCI and NBTI effects.

ELDO CLASSIC—THE CORE AMS TECHNOLOGY

Because Eldo Classic is used as the core technology of Questa ADMS, the tool provides a smooth path to analog and mixed-signal top-down design techniques using SPICE, Verilog, Verilog-AMS, VHDL, and VHDL-AMS languages.



Mentor Graphics Analog/Mixed-Signal IC Design Flow

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