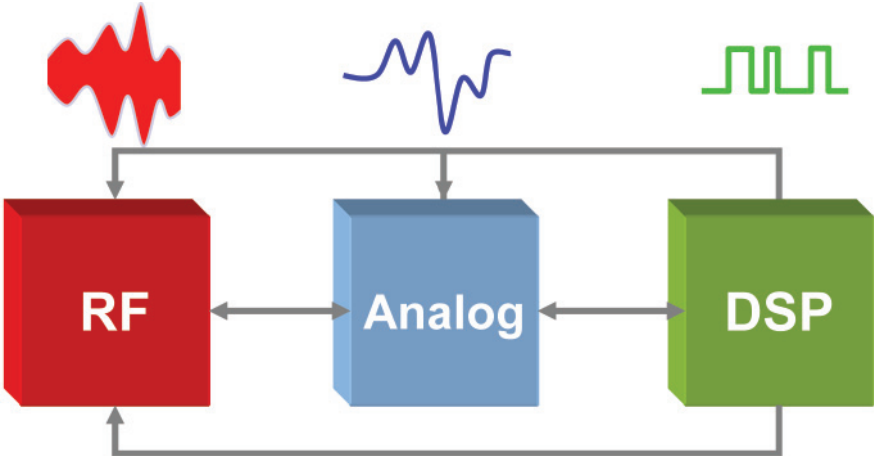
Questa ADMS RF

RF and Mixed-Signal Simulation

Analog/Mixed-Signal Verification

D A T A S H E E T



Questa ADMS RF is a unique simulation solution allowing efficient verification of such circuits. Questa ADMS RF provides 100X or 1,000X speed-up ratios over regular time-domain simulation.

COMPLETE VERIFICATION OF RF-DSP SYSTEMS

Complete simulation of RF system-on-chip (SoC) becomes a reality with the combination of the Eldo® RF capabilities into Questa® ADMS™. Built upon these solid foundations, the Questa ADMS RF solution allows effective simulation of communication systems containing tightly linked radio frequency (RF) and baseband functions—analog and digital.

Questa ADMS RF

Questa ADMS RF targets the simulation of systems integrating an RF front-end and baseband functions with complex digital signal processing (DSP) in VHDL or Verilog. Direct conversion receivers or amplifiers with high-speed digital automatic gain control (AGC) are among the simplest examples. Verifying such systems mandates simulation solutions with which the transistor-level RF part can be simulated simultaneously with the baseband part, in practical CPU time.

BUILT ON SOLID FOUNDATIONS

About Questa ADMS

Questa ADMS is an industry-leading tool for mixed-signal simulation. Complex mixed-signal chips can be verified with all their analog-digital

Key Benefits

- Minimizes risks of faulty RF/baseband connections with more complete verifications of complex RF SoC for wireless communication applications
- Enhances productivity because RF and baseband IC designers can start working together, with the same tools, much earlier in the design process

Key Features

- Uses industry-standard languages only, and no proprietary languages; facilitates reuse of unmodified legacy code
- Simulates complete systems orders of magnitude faster than previous tool generation. Many more operating conditions can be verified
- Preserves transistor-level accuracy wherever necessary

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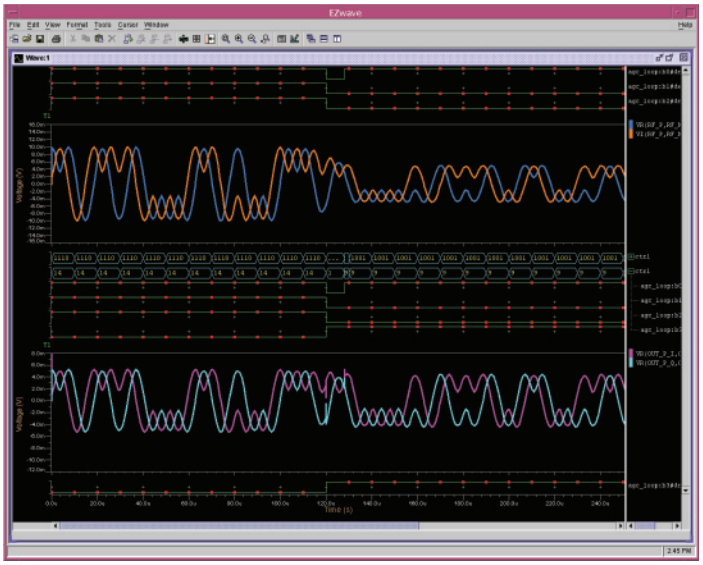
connections. It is a language-neutral environment including SPICE, VHDL, Verilog as well as standard analog behavioral languages such as VHDL-AMS and Verilog-A.

About Eldo RF

Eldo RF provides the necessary algorithms to handle RF blocks efficiently in typical RF transceivers, such as low noise amplifiers, mixers, or voltage controlled oscillators. It features high-performance RF-specific algorithms such as the steady-state analysis and the modulated steady-state analysis (MODSST). This provides the necessary simulation speed-up for these critical blocks operating at the highest frequencies, typically several gigaHertz.



QUESTA ADMS RF—HOW DOES IT WORK ?

Questa ADMS RF uses the MODSST algorithm of Eldo RF in place of the transient algorithm of Questa ADMS. The circuit is described with any mix of SPICE, Verilog-A, VHDL-AMS, Verilog, and VHDL.

The MODSST algorithm is a mixed time-frequency algorithm that computes a time-varying spectrum. At discrete time points, the spectrum of the signals is computed using the steady-state analysis of Eldo RF. The spacing of time points is chosen to follow the slow-varying baseband information, rather than the fast-varying RF carriers.

This results in huge speed-up ratios over regular transient simulation. Two or three orders of magnitude are usual with the typical baseband-to-carrier frequency ratios in wireless networks applications.

Single Kernel Architecture for RF-DSP Simulation

Questa ADMS RF is a straightforward extension to the single-kernel architecture of Questa ADMS and thus greatly simplifies the usage of its complex underlying algorithms.

This architecture radically departs from so-called co-simulation approaches where foreign simulators are glued together, using limited and cumbersome interfaces.

It allows you to concentrate on design issues only, not simulator issues. The usual Questa ADMS interface is left unchanged, and the Eldo RF MODSST analysis is used in place of the usual transient analysis.

Transistor-Level Accuracy

Questa ADMS RF differs radically from “system-level” approaches, which rely on behavioral modeling based on proprietary languages or even simple linearization of the fast-varying RF signals. Questa ADMS RF retains the full accuracy of circuit-level simulation, where and when you want it to.

The critical RF blocks can be described in SPICE, so that all high-order effects are still captured (popular foundries deliver device model parameters for Eldo, based on the Bsim3, Bsim4, PSP, or HICUM standards). For increased performance, less critical RF or analog blocks can be described in Verilog-A or VHDL-AMS, and all the DSP can be described in Verilog and/or VHDL.

Digital Modulation for All Wireless Standards

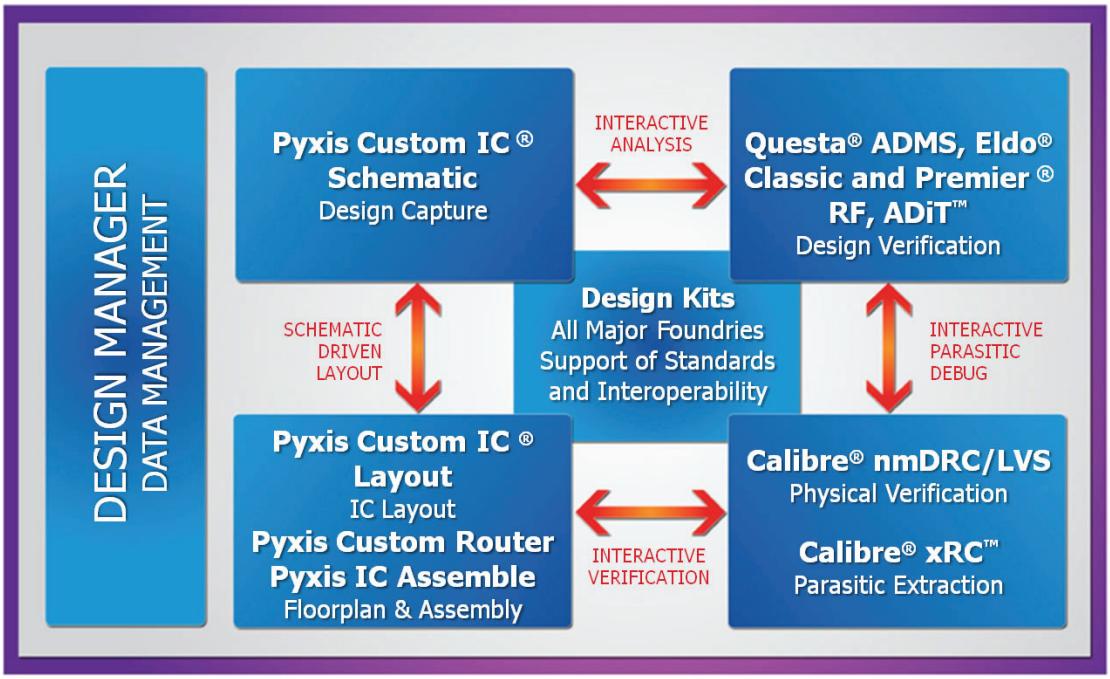
To simplify simulations in the context of wireless standards, Questa ADMS RF supports all common digital modulation formats, such as GMSK, QPSK, QAM, GFSK, EDGE, HPSK, OFDM, etc. Built-in sources deliver signals modulated according to these schemes, including the standard baseband filters such as root cosine or Gaussian filters. The input signal can be either explicit binary sequences or CCITT-compliant PRBS sequences.

Questa ADMS RF displays IQ constellation diagrams and trajectories, Eye diagrams, CCDF, modulation spectrum etc. Measurement functions allow estimating critical figures of merit such as, ACPR, EVM, or BER.

MAXIMIZE REUSE FOR MORE PRODUCTIVITY

Questa ADMS RF uses industry-standard languages only: SPICE, VHDL, Verilog, Verilog-A and VHDL-AMS. Reuse of legacy code is thus greatly simplified. An existing Questa ADMS design can be imported in a matter of seconds, without any modifications, and simulated along the transistor-level mixers and VCOs of the RF front-end, whatever the feedback and control loops.

Questa ADMS RF is integrated in the Mentor IC Flow and also in the Cadence® ADE framework.



Mentor Graphics Analog/Mixed-Signal IC Design Flow

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Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070-7777
Phone: 503-685-7000
Fax: 503-685-1204

Sales and Product Information
Phone: 800-547-3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

North American Support Center
Phone: 800-547-4303

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1001, 10F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-87252000
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140 -0001
Japan
Phone: 81-3-5488-3033
Fax: 81-3-5488-3004

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