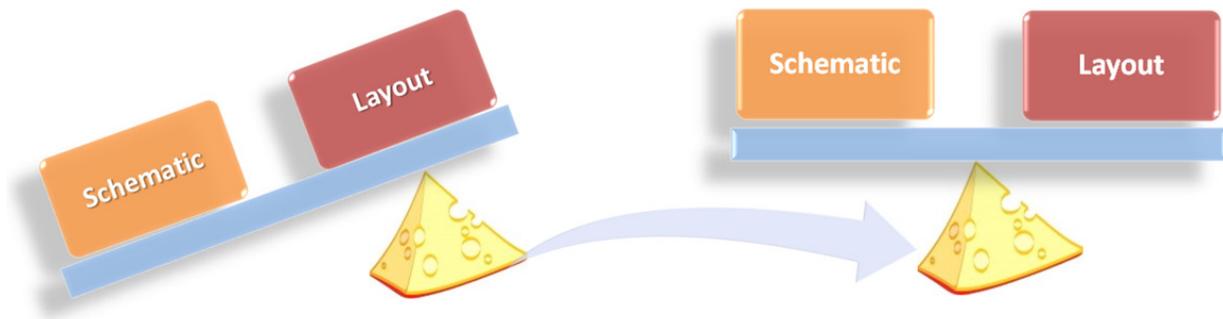


# The Si-Cheese is moving...

## Why the Reconciliation of Electrical and Physical Effects is Critical to Future AMS Designs



Over the years, the continuous downscaling in CMOS technology has been the main ingredient enabling the rapid evolution of electronic applications. Nurtured by incessant research and bounteous industrial funding, miniaturization of silicon has constantly allowed for faster switching and, hence superior, digital computing capabilities.

Based on this seemingly solid promise, the electronics market has rapidly grown both in size and demands. Today, high-speed mixed-signal applications have become greedy in terms of power and speed levels that can be sustained by a silicon die.

Achieving chip sign off, particularly for mixed-signal chips, is becoming an increasingly

complicated task using sub-45 nm technologies. The intricacies involved are mainly driven by the silicon roughness prominent at such small geometries.

Recently, technologists demonstrated STI-related stress to severely disrupt the electrical characteristics of MOS devices. This also gives rise to various deleterious layout dependent effects (LDEs) that affect the device's intended performance and subsequently upset system functionality. For this reason, careful handling of these effects at advanced process nodes is necessary to guarantee the design's robustness.

It follows that this auxiliary effort renders the design process more convoluted, eventually threatening meeting time-to-market.

Dragged by the digital thirst for faster gates, coexistent analog content undergoes the toughest challenge to tame the agitated silicon. At nanometer process nodes, analog behavior is highly sensitive to layout interdependencies that rapidly cause intolerable device mismatch—a 20% shift in threshold voltage is a common example if LDEs are not carefully accounted for.

Today's class of EDA tools does little to help preserve the designer's intent against these types of complexities.

What is needed is layout-aware schematic-level design methods and tools that allow designers to access and analyze transistors non-idealities caused by the proximity of

neighboring devices and structures in the layout.

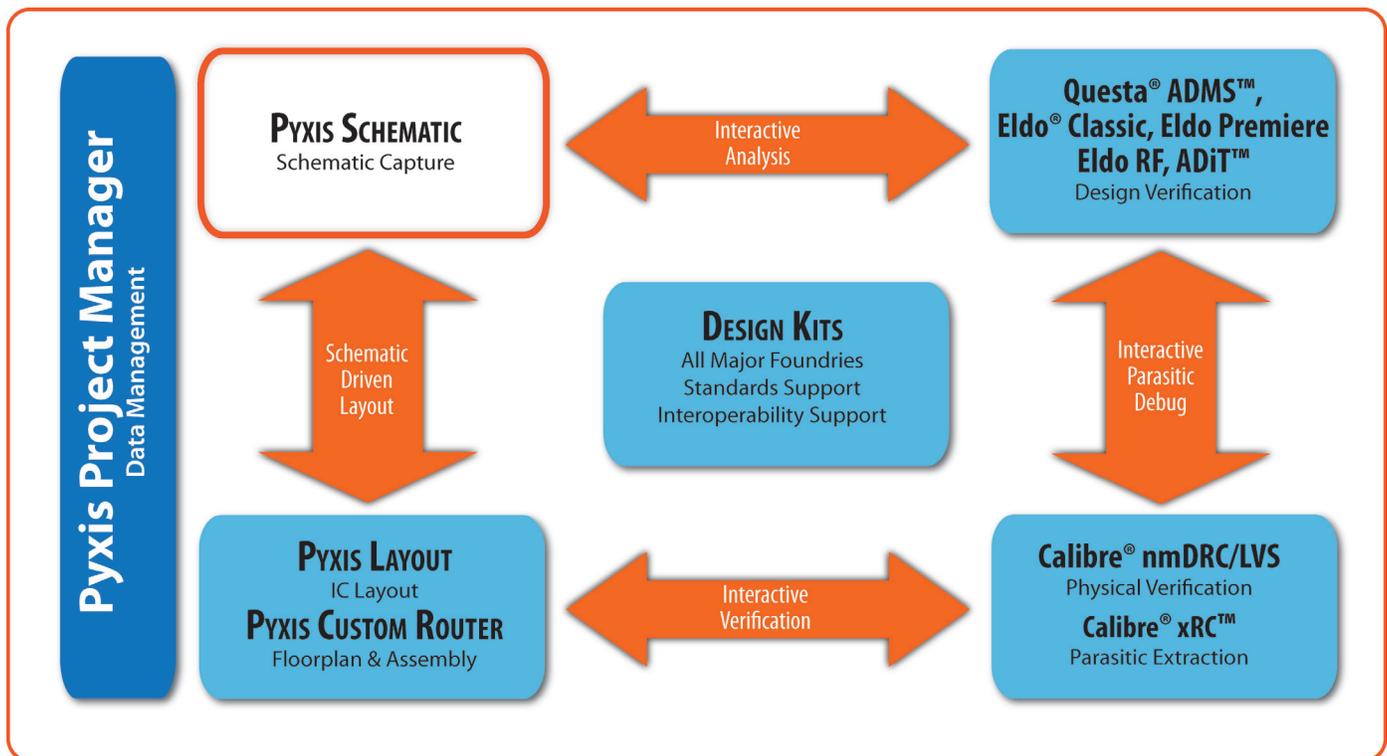
Eventually, we must evolve parametric/electrical sign-off to reduce cost and ensure yield at these deep submicron levels.

Moreover, to achieve parametric yield at 28 nm and below,

analog designers cannot wait until post-layout verification to analyze layout -dependent effects. Instead, a fusion between electrical and physical effects is needed during the early circuit design cycle.

Visit us at [www.mentor.com/dsm](http://www.mentor.com/dsm) to find out more about Mentor Graphics deep submicron EDA tools for the analog/mixed-signal and custom IC industries.

## Mentor Graphics Analog/Mixed-Signal IC Design Flow



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**Corporate Headquarters**  
Mentor Graphics Corporation  
8005 S.W. Boeckman Road  
Wilsonville, Oregon  
97070-7777  
Phone: 503-685-7000  
Fax: 503-685-1204

**Silicon Valley**  
Mentor Graphics Corporation  
46871 Bayside Parkway  
Fremont California 94538 USA  
Phone: 510-354-7400  
Fax: 510-354-7467

**Europe**  
Mentor Graphics Deutschland GmbH  
Arnulfstrasse 201  
80634 Munich  
Germany  
Phone: +49.89.57096.0  
Fax: +49.89.57096.400

**Pacific Rim**  
Mentor Graphics Taiwan  
Room 1001, 10F,  
International Trade Building  
No. 333, Section 1, Keelung Road  
Taipei, Taiwan, ROC  
Phone: 886-2-87252000  
Fax: 886-2-27576027

**Japan**  
Mentor Graphics Japan Co., Ltd.  
Gotenyama Garden  
7-35, Kita-Shinagawa 4-chome  
Shinagawa-Ku, Tokyo 140 -0001  
Japan  
Phone: 81-3-5488-3033  
Fax: 81-3-5488-3004

**Sales and Product Information**  
Phone: 800-547-3000

**North American Support Center**  
Phone: 800-547-4303

