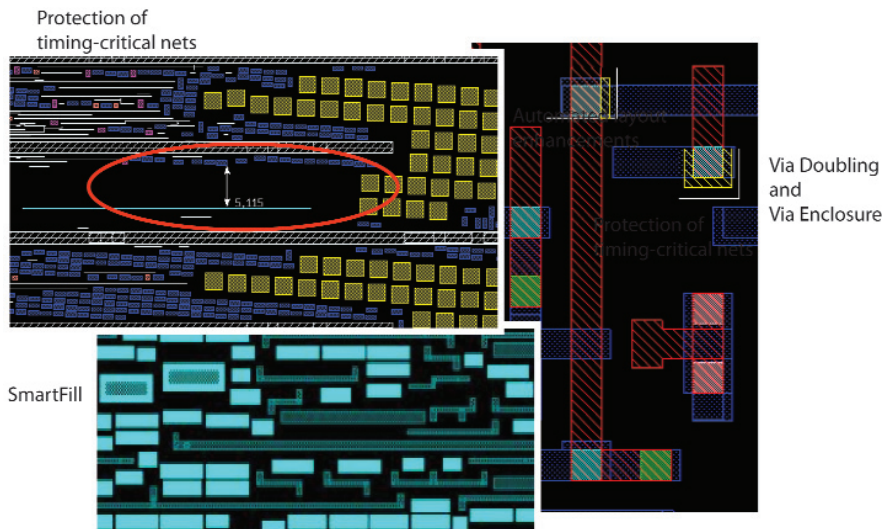


# Calibre YieldEnhancer



*Calibre YieldEnhancer automatically modifies the layout to improve robustness of the design and yield. Modifications are inserted back into the design database.*

## Calibre YieldEnhancer

Calibre YieldEnhancer is part of the Calibre Design-to-Silicon platform, and is a natural extension of the Calibre Standard Verification Rules Format (SVRF) language. While designers may use SVRF to do their own layout enhancements and output modifications to GDSII or OASIS format, Calibre YieldEnhancer expands this capability in two ways.

First, it uses built-in functions optimized to maximize coverage and minimize run times. Calibre YieldEnhancer provides the functionality to add a smarter fill, automatically double vias, and expand/extend metal enclosures. For example, via doubling supports multiple via patterns. When comparing Calibre YieldEnhancer against user-defined via doubling SVRF code, designers have seen the number of vias increase by 4-10%, while reducing runtimes between 5-15X.

Second, Calibre YieldEnhancer gives designers the best of both worlds: the industry's most powerful layout modification environment that also fits into industry-leading design environments. As new problems are discovered, users need to respond quickly to the types of layout modifications that are required to improve yield. Calibre YieldEnhancer will continue to support user-defined enhancements and facilitate that capability through back-annotation of the changes into industry standard databases, such as OpenAccess® or Milkyway®.

## Automated Layout Modifications

With the progression of complex, high-performance nanometer designs, design robustness and acceptable yield have become difficult to attain. While manufac-

### Key Product Benefits

- Automatically modifies the layout to improve design robustness and yield
- Evolutionary fill solution provides path from dummy fill all the way to model-based fill
- Integrated with industry-standard databases such as OpenAccess® and Milkyway®
- Leverages the common Calibre interface for easy and fast adoption, and Calibre Interactive of push-button access from the design framework
- Fully integrated with the Calibre tool suite and popular layout environments

### Key Product Features

- Transition between fill solutions without changing tools
- Automated via doubling, via extensions, and via enclosures
- Back-annotation of user-specific layout modifications
- Integrated with Calibre RVE and Calibre DESIGNrev for visualization
- Integrated with Calibre Interactive for push-button access from the design framework

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turers have traditionally handled yield management, more pressure is being placed on designers to adopt design for manufacturing (DFM) methods that help ensure manufacturing success. Mentor Graphics provides a comprehensive suite of products that work together to improve design robustness and yield. As part of that product suite, Calibre® YieldEnhancer provides automated layout modifications to enhance the design.

Calibre YieldEnhancer provides three types of automated layout modifications: SmartFill technology to handle a variety of fill solutions, via modification (including via doubling and expanding the metal over the vias), and programmable edge modification. To improve yield and design robustness without sacrificing area, Calibre YieldEnhancer seeks to take advantage of any white space when applying these layout modifications. To balance performance, Calibre YieldEnhancer offers both a net-aware capability and back annotation to the design database. Calibre YieldEnhancer works with Calibre YieldAnalyzer and Calibre CMPAnalyzer to measure the impact of layout modifications.

### **“Smart” Automated Fill Algorithms**

The first automated fill solution, known as “dummy fill,” provides a simplistic fill algorithm based on foundry density specifications. Fill solutions become more challenging with each smaller node because manufacturing processes and physical interactions become more sensitive to metal density variations. In addition, the performance of the chip becomes more sensitive to parasitic capacitance (which is increased by adding metal fill) and variations in interconnect resistance (due to CMP impact on metal thickness). As designs become more complex, and feature sizes shrink, meeting all of these constraints requires better analysis to predict the manufacturing and electrical impacts of fill, and more sophisticated algorithms that optimize the use of metal fill features.

Calibre YieldEnhancer’s SmartFill technology combines density analysis with the filling operation to minimize the number of fill shapes added. Additionally, it provides such advanced capabilities as multi-layer fill shapes, and support for non-rectangular fill shapes to optimize performance of the fill. Because density goals and analysis are included in the SmartFill algorithm, the filling procedure is stopped when SmartFill reaches the density constraints, which include min, max, gradient and magnitude. The goal of SmartFill is to achieve adequate fill density with significantly

fewer shapes than dummy fill.

SmartFill is designed to take multiple types of constraints, including Calibre’s unique equation-based design rule specifications. This capability enables designers to analyze fill solutions using continuous, multi-dimensional functions in place of linear pass-fail conditions. These design rule equations can enable finer resolution of complex fill rule checks that cannot be performed with single-dimensional design rules alone. Equation-based fill allows users to account for other effects besides density. This combination also provides users with a transition from a density-based solution to a model-based approach, by enabling them to consider 1st order effects other than density.

For the most specific and customized fill solution possible, SmartFill uses information obtained from Calibre CMPAnalyzer that is derived using algorithms based on thickness simulation data from a full CMP simulation. SmartFill uses this data to determine the optimum filling strategy. The combination of accurate simulation data and the innovative Calibre fill algorithm improves parametric yield by reducing thickness variation that affects resistance, while at the same time minimizing the capacitance added to the design. Model-based fill enables designers to add as few shapes as possible while still achieving specific planarity goals.

### **Via Enhancement**

There are two design issues that can impact robustness of design and contribute significantly to potential yield loss: 1) the number of single vias, and 2) the number of via transitions with minimal overlap. However, applying a blanket rule that every via must be doubled results in area penalty that most designs cannot afford. Calibre YieldEnhancer automatically evaluates every single via, and uses a powerful array of configurations to maximize the number of vias doubled without affecting area while also minimizing run time.

Calibre YieldEnhancer performs multi-layer operations that support multiple configurations that maximize the coverage and minimize jogs. These operations include both edge modifications based on multi-layer checks (such as enclosure and extensions rules), and single-layer grow operations. Layout modifications remain DRC-clean while taking advantage of as much white space as possible.

## Programmable Edge Modifications

For advanced design teams that can identify ways to improve the robustness of their design through edge movement, Calibre YieldEnhancer provides a unique way to modify the layout. This is especially true for technologies going through the yield ramp phase. Because these design teams cannot wait for an EDA vendor to provide a generic solution, Calibre YieldEnhancer provides programmable edge capabilities that are unique in the industry.

Designers assign (through analysis) the amount of modification, and they assume the responsibility for ensuring the modifications will be DRC-clean. Once they decide how much to move an edge or resize a polygon, they simply assign a property to that design element. This property provides direction to Calibre YieldEnhancer to enable it to make the modification. The property assignment is performed with equation-based DRC (eqDRC), a unique and innovative technique within Calibre nmDRC.

## Area/Yield Tradeoff

To make the area/yield trade-off, Calibre YieldEnhancer focuses on taking advantage of white space. Layout modifications are made if they can improve yield without increasing die area. Calibre nmDRC, the industry standard in physical verification, provides the flexibility to move from the minimum DRC rules toward the recommended values. Because Calibre YieldEnhancer is integrated with the Calibre platform, users can be confident that the outcome is DRC-clean. Calibre YieldEnhancer provides as much layout modification as possible without creating DRC violations.

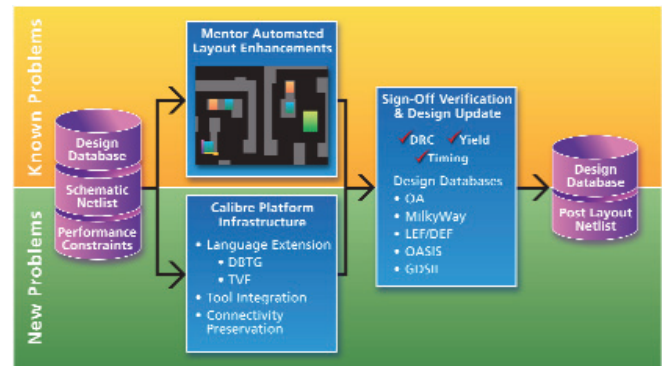
## Ensuring Performance

Performance is another critical factor that designers need to balance. It is important to limit the impact of DFM modification on the final timing. Calibre YieldEnhancer uses a two-prong method for dealing with timing. First, designers can simply provide a list of critical nets that are timing-sensitive. This list ensures that no vias are added on these timing-critical nets. In this case, additional via coverage is sacrificed to reduce the impact on timing. Second, Calibre YieldEnhancer enables the back-annotation of the yield modifications to the designer's database, so users can easily verify timing, power, and signal integrity with their standard procedures.

## Calibre DFM Platform

Calibre is the sign-off standard at a majority of the world's foundries, and offers a comprehensive set of tools that address the complex handoff between design and manufacturing. The Calibre platform also acts as the conduit for a DFM feedback loop. Calibre YieldEnhancer not only produces DRC-clean results, but also works with Calibre YieldAnalyzer to provide a before and after view of the yield improvements.

Calibre YieldAnalyzer combines critical area and recommended rules into a signal analysis package. Both tools leverage the interface tools of Calibre, which include Calibre Interactive for job submission, and Calibre RVE (Results Viewing Environment) for displaying the output within industry design tools.



*Calibre YieldEnhancer is a layout modification platform that provides automatic layout modifications or allows users to create their own modifications, while managing database integration.*

## The Calibre nm Platform

Calibre YieldEnhancer is built on the Calibre nm platform, the industry's leading physical verification platform, known for delivering best-in-class performance, accuracy, and reliability. A powerful hierarchical engine is at the heart of the Calibre tool suite, which offers a complete IC design-to-manufacturing solution. In addition, Calibre MT, Calibre MTflex and Hyperscaling enhance performance and reduce turnaround times across the platform.

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## Expert Consulting Services

As a Calibre user, you also have access to Mentor Graphics yield enhancement consulting services. Mentor Consulting Design Enablement and Customization Services provide the expertise and project management skills required for effective deployment of advanced technologies. Our consultants can quickly get you up to speed in your environment and on the path to better performance and improved productivity.

## Superior Product Support

Mentor Graphics is the only EDA vendor to receive the Software Technical Assistance Recognition (STAR) Award in



EDA for technical support excellence FIVE times. For this achievement, Mentor Graphics was inducted into the STAR Hall of Fame. No other provider of complex software can match

the support offered by Mentor Graphics.

## Industry Support

Mentor Graphics Calibre technology is widespread through the industry. This relationship with your manufacturers makes the decision to use Calibre technology the lowest risk choice.

**Visit our website at [www.mentor.com/](http://www.mentor.com/)**

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