# Optimizing Yield

# Using equation based DRC (eqDRC)

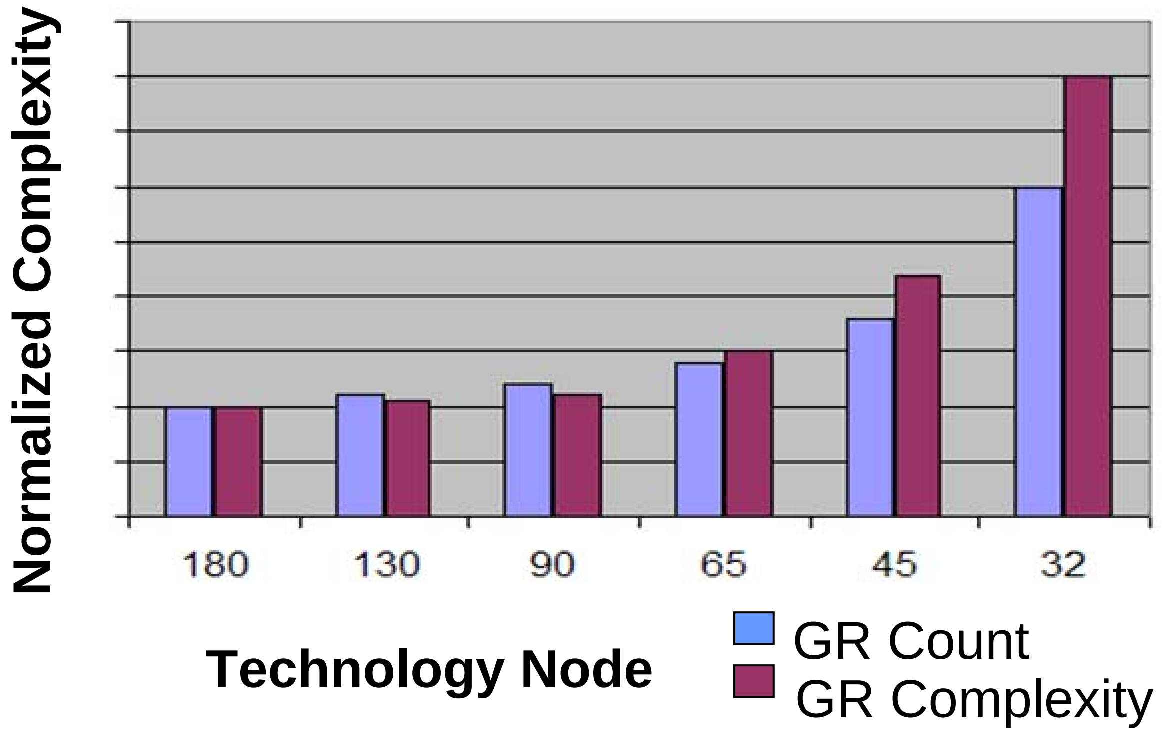
## A focus on Circuit Limited Yield (CLY)

# Agenda

- **Overview and Motivation**
- **Circuit Limited Yield, what it means**
- **How IBM uses eqDRC to analyze for CLY - Measure**
  - NW Scattering exampe
  - Code breakdown
- **Using eqDRC to improve designs - Model**
- **Using eqDRC to improve yield - Mitigate**
- **Conclusions**

# Industry forecast- Increasing Design Complexity

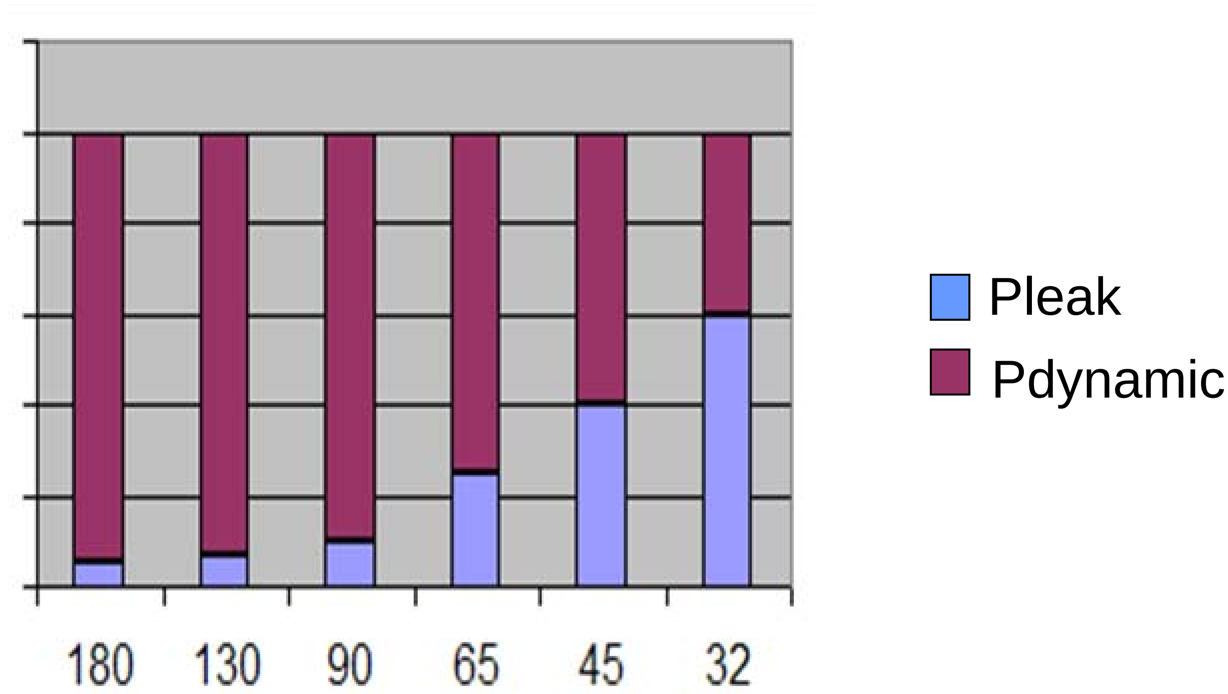
- **With Each technology node, both the number and complexity of rules increases.**
- **Implementation of physical design and design rule checking advances has been stymied because of tool centric behaviors.**




- **This increasing trend is intended to properly balance the costs of increased design complexity and the increased number of forecast yield detractors.**
  - Low K1 litho
  - Pleak vs Ptotal
- **This is a delicate balance and must be made years in advance of the first products received in a technology.**
- **EqDRC can and will certainly limit this growth by combining table-based and complicated rules into analytic forms that are easier to understand and maintain.**

# Industry forecast – $P_{leak}$ Increasing percentage of $P_{total}$

- **Each generation has seen leakage power comprising a greater percentage of total power.**

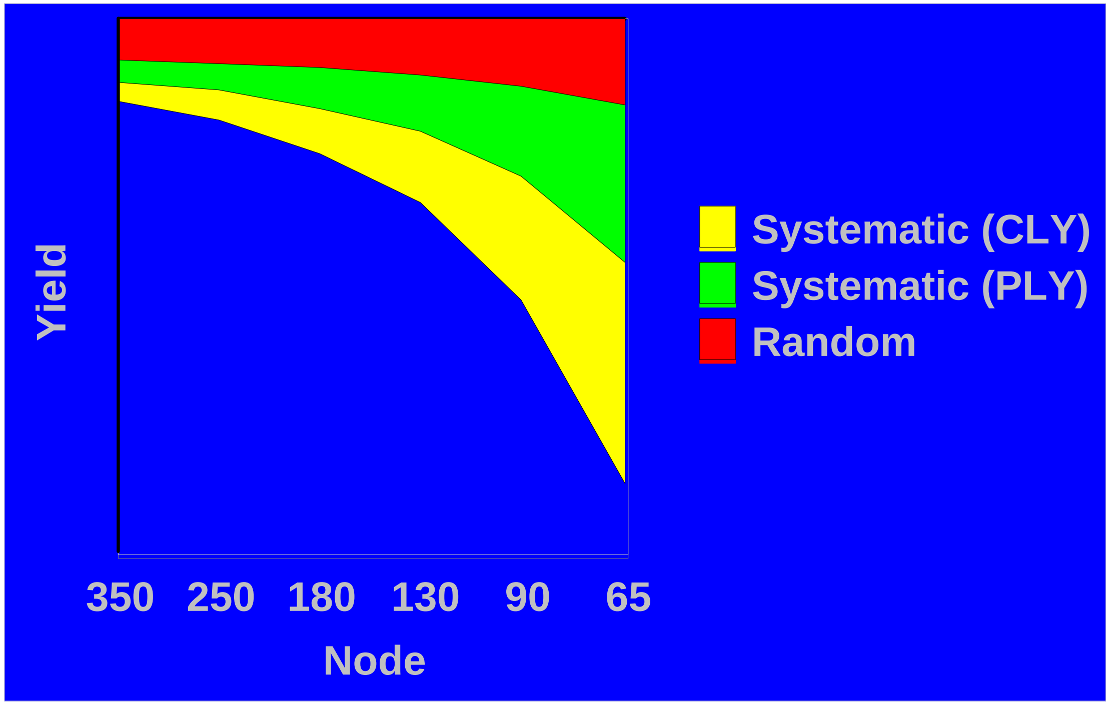



•As a result, any inability to control or predict the impact of Leakage power variation results in reduced margin.

# Industry Forecast - Circuit Limited Yield (CLY)

- **<u>Problem Being Addressed:</u> Foundries have limited visibility into a given parts susceptibility to power or frequency deviations from functional specs.**

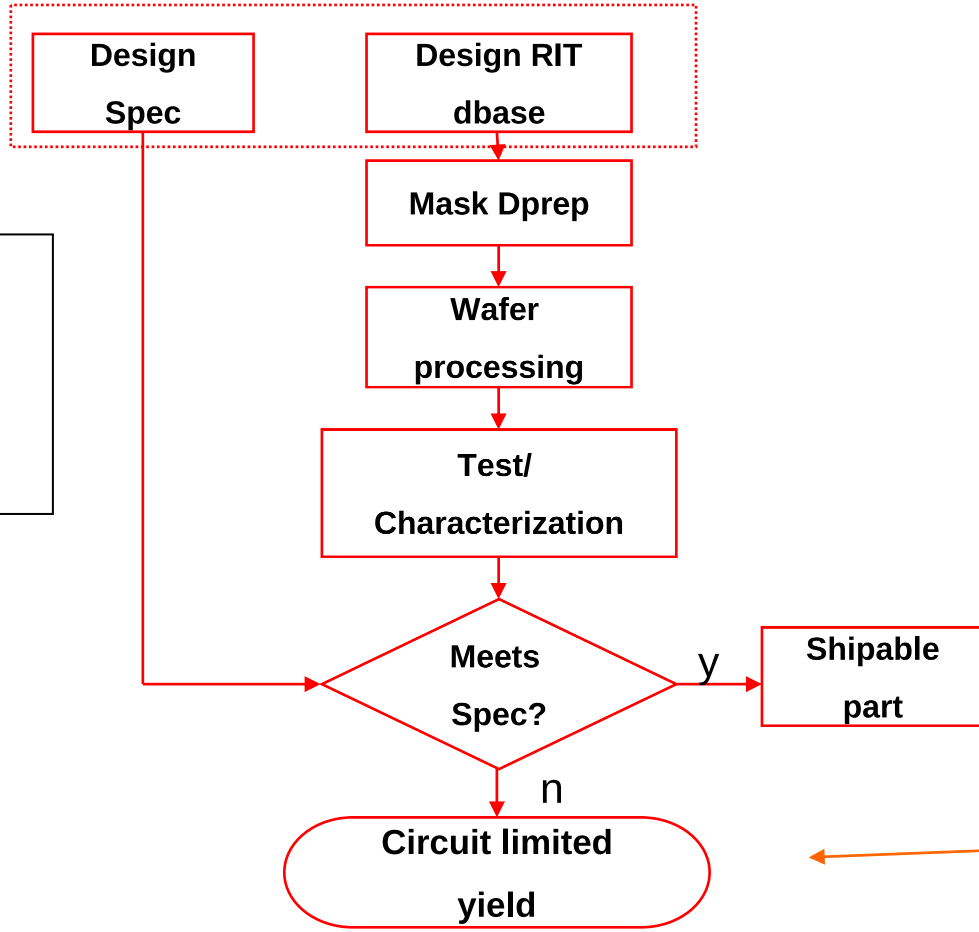
- Design Intent conventions will further enable CLY mitigation




- **CLY is viewed differently by designers and by manufacturing Fabs.**
  - Design –
    - CLY requires increased guard banding. Technology capability can't be fully realized.
    - CLY is Manufacturing's problem, design pays for chips below power and at frequency
  - Foundry – CLY reduces margin, and can't be predicted independently.
    - **Manufacturing currently has limited capability to even qualitatively assess the CLY potential for two arbitrary designs**.
    - Iddq and fmax prediction require additional design information (or do they?).
    - Most of the design intent information is lost during design submission.
    - **<u>Significant potential exists now for CLY optimizations in manufacturing</u>**.

# CLY - Measure

Where we are without CLY prediction and mitigation tools and techniques




unacceptable risk
$$$

**Fab has limited/no**

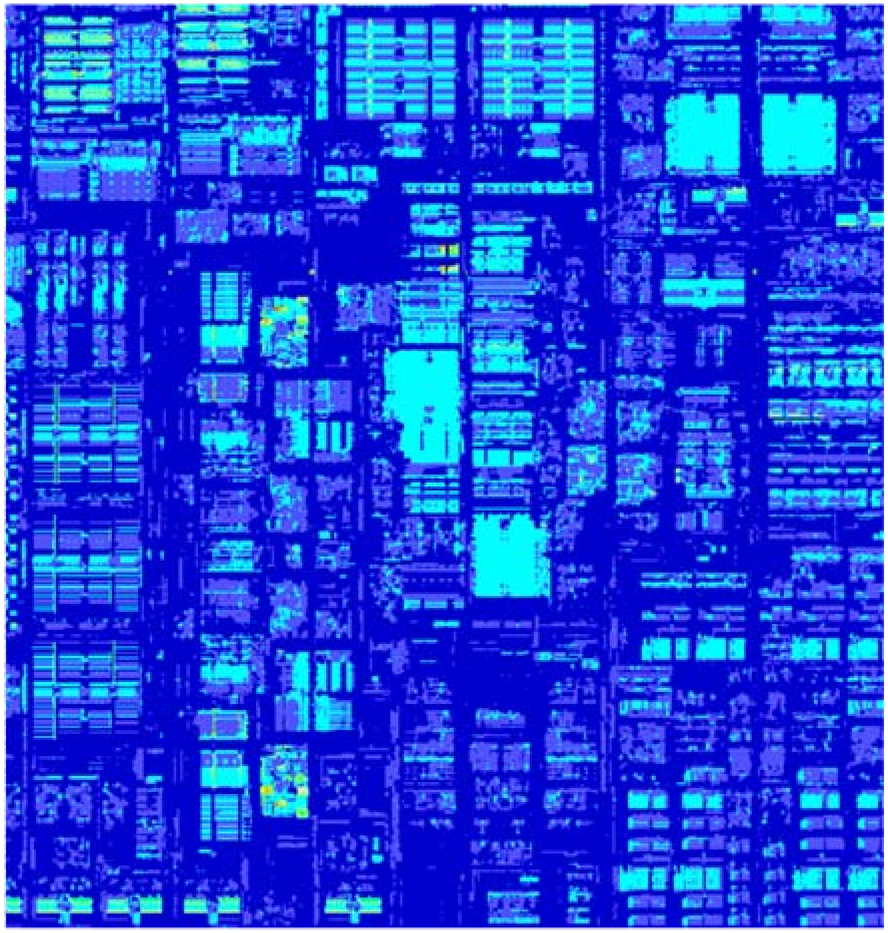
**Ability to investigate, model**

**Or mititgate**

**Source of CLY**

# So, what can we do about it??

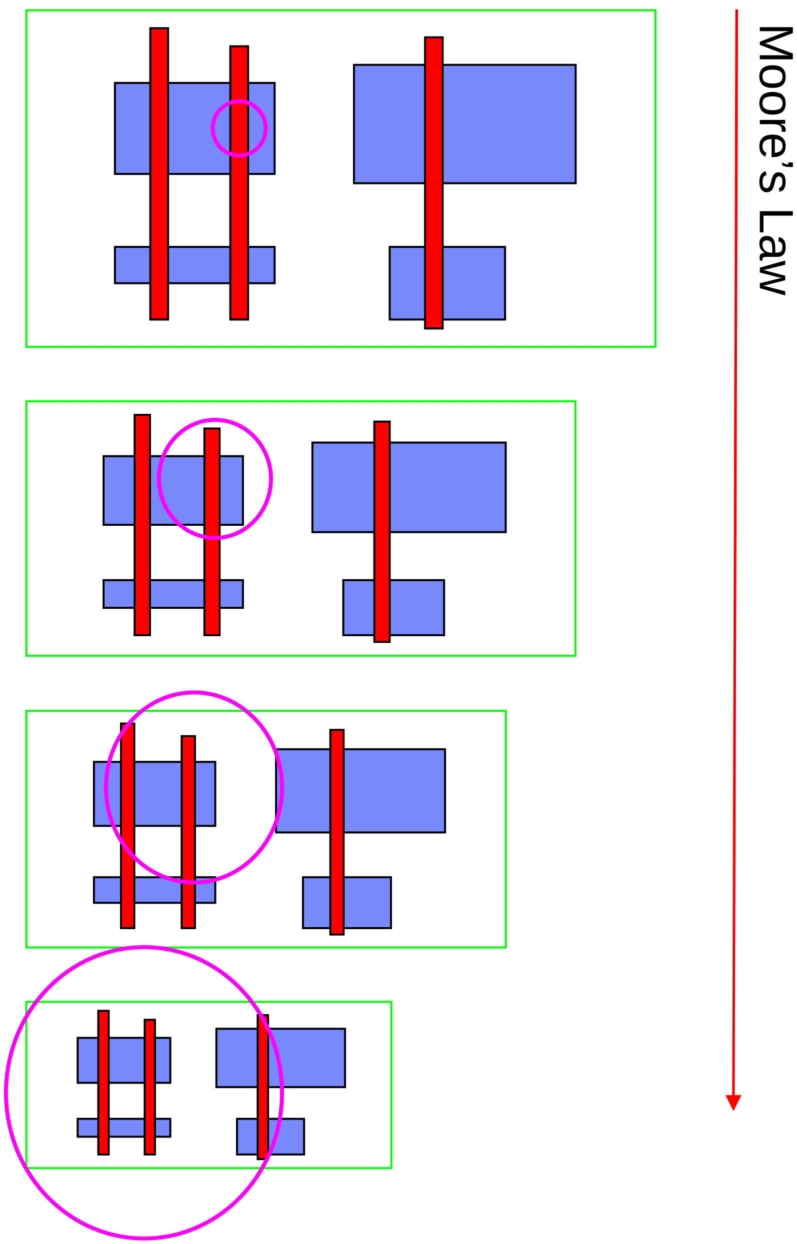
- **Currently, eqDRC provides CLY predictions using**
  - GateSpace stats
  - GateWidth Stats
  - GateLeff stats
  - SA/SB stats
  - NWscattering stats (example follows)
  - CR stats
  - Device type and count numbers
  - Gate Area stats
  - Calculations of Iddq nominal
    - With NW proximity
    - With NCE
    - With CR, and pitch
    - By cell
    - Full chip
    - By region
  - Calculations of Idsat also include stress variants



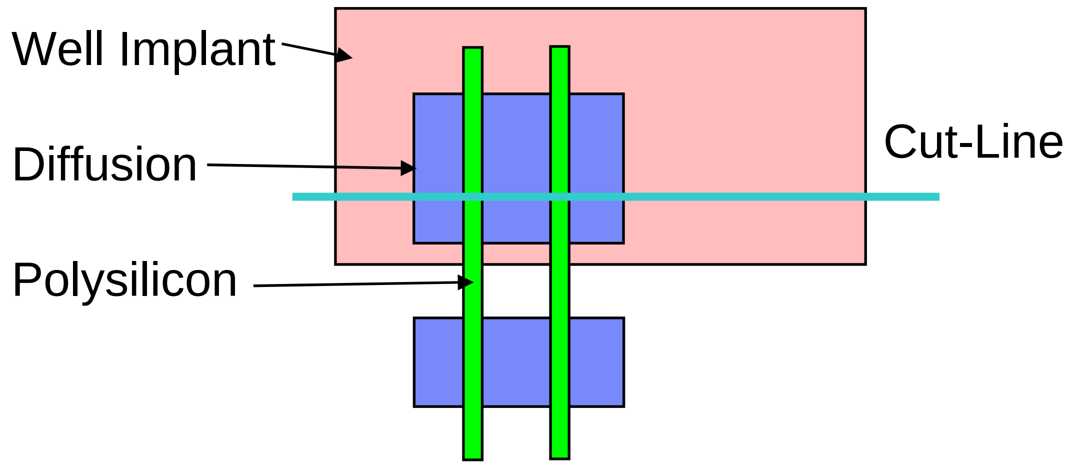
Full Chip Iddq Prediction and Map

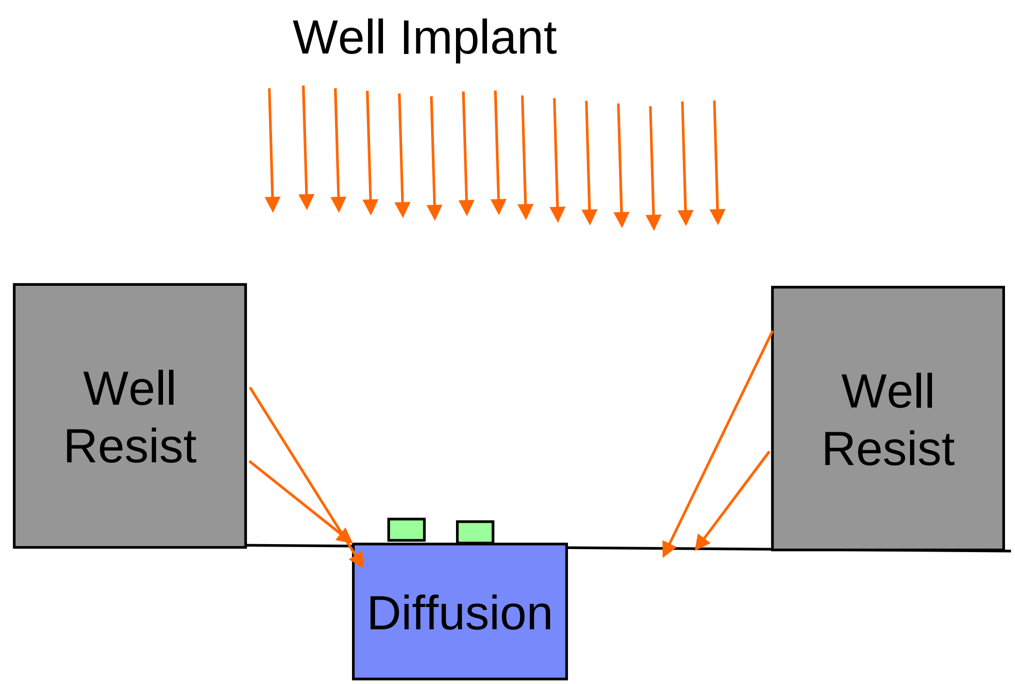
# Why it's useful

- In previous technologies, the physical phenomenon impacting performance were localized within the cell.
- With each subsequent generation, the cells scaled, but the phenomenon often remained the same or grew in comparison.
- This results in many phenomenon that lie beyond the range of the cell boundaries and are not be accounted for during cell characterization.
- With each subsequent generation, the number and extent of these variations increases contributing to the yield trend chart on page 4.
- EqDRC enables this detail to be analyzed at full chip level and reported with granularity that the user specifies.



- **This is a well known and modeled phenomenon called NW scattering.**
- **It results from ions scattered off resist walls into nearby diffusions**
- **It is higher if the device is smaller and if the NW distance is lower.**



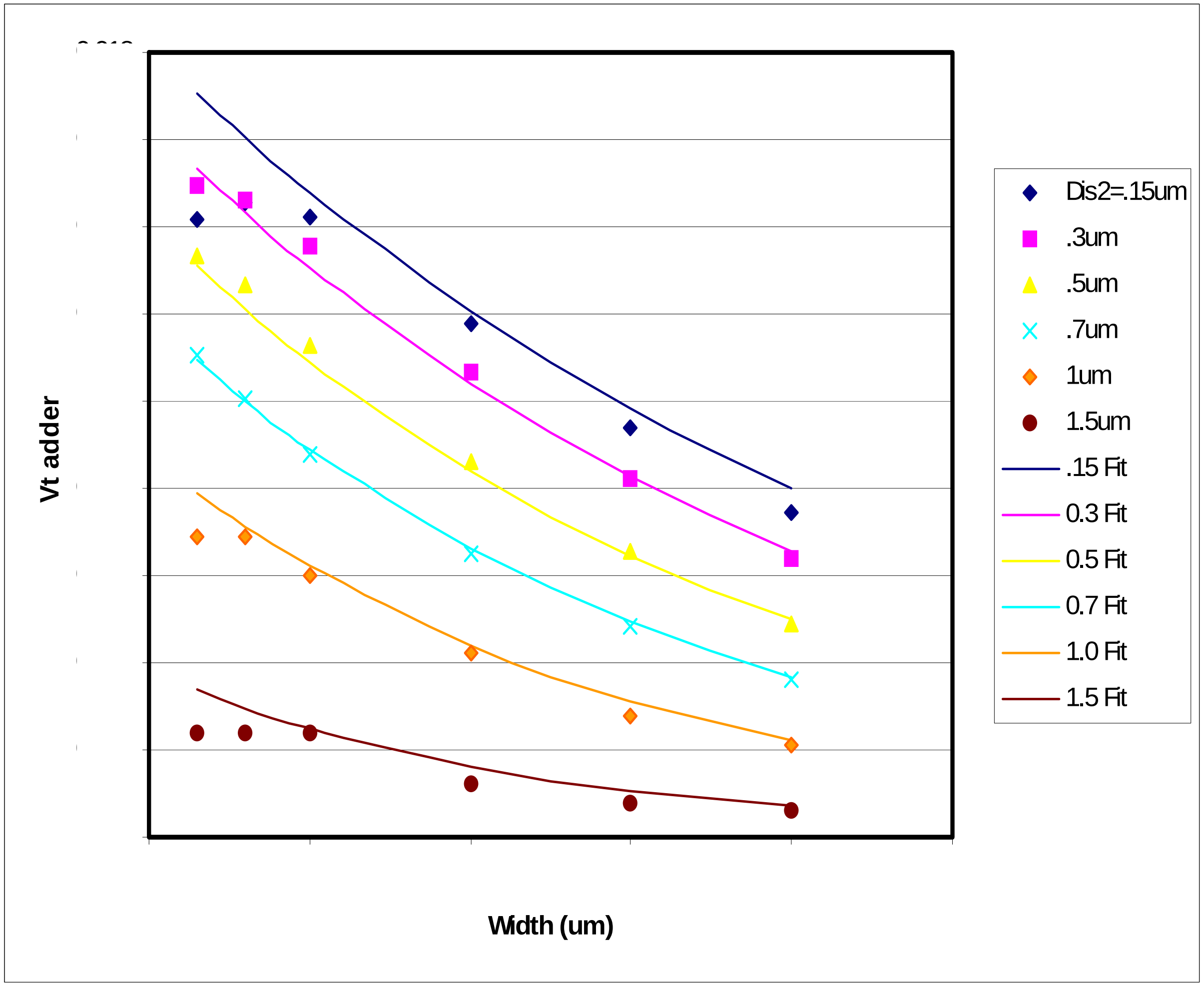



We calibrate eqDRC using compact model forms to BSIM or other process models

$$VtAdd = f(W, Dis)$$

$$VtAdd = a_o + a_1 e^{w} + a_2 w e^{w} + a_3 e^{Dis} + a_4 Dis e^{Dis}$$

- **This model is implemented with eqDRC**
- **Each gate gets measurements for NW proximity and gate.**
- **Vt add is calculated for each NW space then summed over the gate**
- **Iddq is calculated for each gate with and without the Vtadd offset and summed over each gate**
- **Iddq is then summed for each cell, full chip and region.**
- **Severity sorting can be done the same way.**



# How We do it…NW scattering example

$$VtAdd = a_o + a_1 e^{w} + a_2 w e^{w} + a_3 e^{Dis} + a_4 Dis e^{Dis}$$

- **Any Arbitrary model form is expressible with eqDRC**
- **VtAdd = DFM PROPERTY Gate W Dis**

  **OVERLAP ABUT ALSO MULTI**

  **[VtAdd=a0+a1*exp(Property(W,W)+**

  **a2*Property(W,W)*exp(Property(W,W))+**

  **…..]**
- **VtAddMap=DFM ANALYZE VtAdd [Property(Vtadd,Vtadd)] >0**
  - Find regions of chip that may be higher then other regions
  - useful for identifying design methodologies that can be problematic.
- **This allows all phenomenon to be combined into a single metric giving a clear signal on needed direction.**

# Used to Improve Physical Design

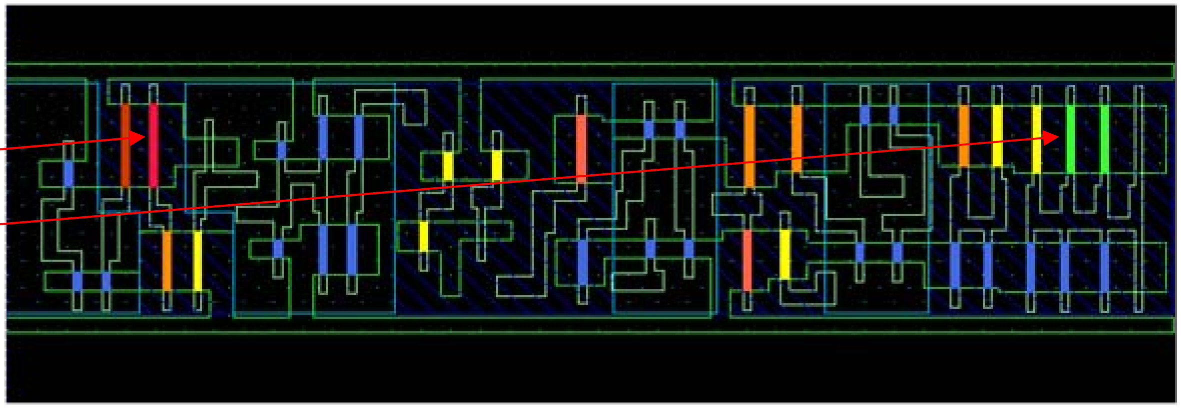
- **Tools using equation based DRC can model systematic sources of current variation.**
- **Each gate and it's surrounding environment is analyzed and scores are assigned according to a model**

$$IdsatIndex = \Sigma \alpha n \Delta P \mathrm{n}$$

$$IddqIndex = \Sigma \beta n \Delta P \mathrm{n}$$

- **Each phenomenon ΔP is scored separately**
  - Each n: Through pitch Across Chip Line Width Variation (ACLV), N-Well scattering, Narrow channel effect, Corner Rounding Stress have both a relative effect, and an effect due to their physical design.
  - Relative importance of different phenomenon are established by coefficients α and β
  - Total results for each gate is the summation in 1 or 2 respectively.
  - Each cell is summed providing a total variability score, and sorted by severity
- **Feedback will guide designer to a less variable layout, while focusing on the most significant detractors first.**

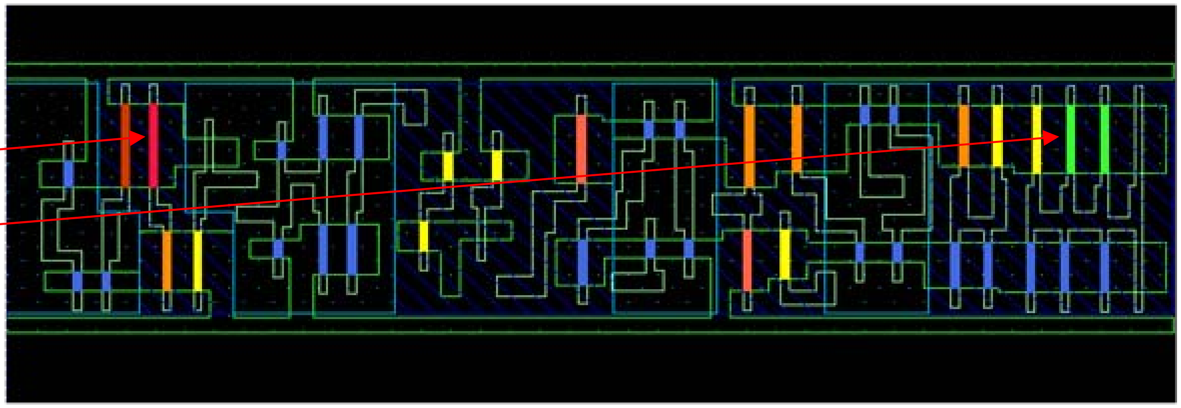
Most Variable Gate (Red)
Least Variable Gate (Green)
(shown for IddqIndex)



# In this way, semi-empirical and analytic models are employed to communicate variability to design or to manufacturing teams

- The within chip sources of parametric variation are calibrated, and each gate is scored based on it's schematic intent Ion/off (from W and L), and it's physical Ion/off for all phenomenon impacting Ion.
  - **Separate indices for Nominal and Process Window (PW)**
- Score a cell by summing the indices over all gates in the cell.
  - Feedback to designers based on Index severity, so the worst cells and gates are corrected first
- Score a chip by summing over all cells
  - Feedback to manufacturing teams and Design teams during design closure.
  - In this manner, a part can be scanned for the cells most likely to suffer from model to hardware miscorrelation
- **In this manner the physical design alone can be used to predict CLY**

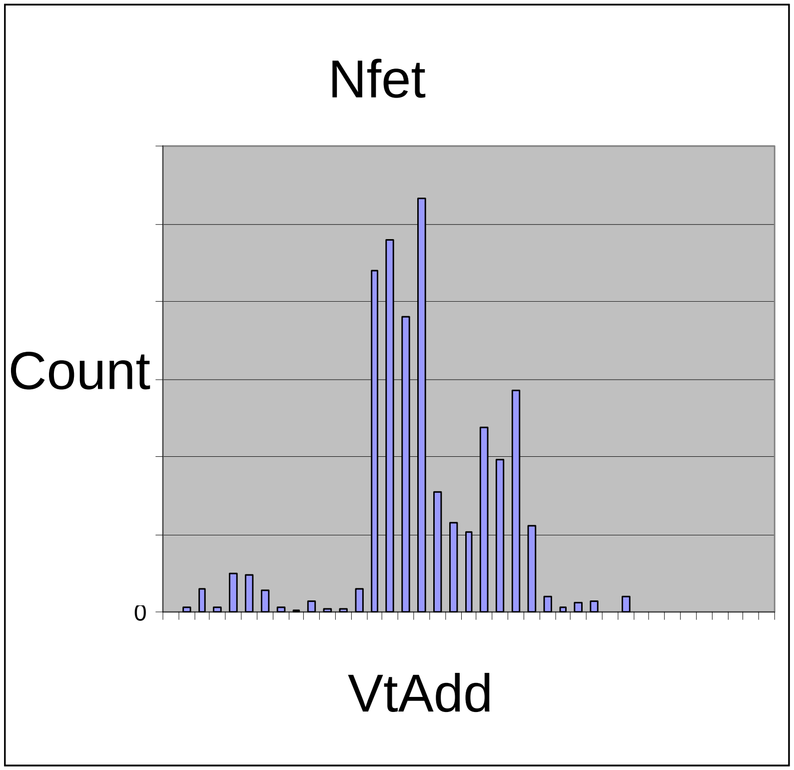
Correct These First (Red)
Correct these last (Green)

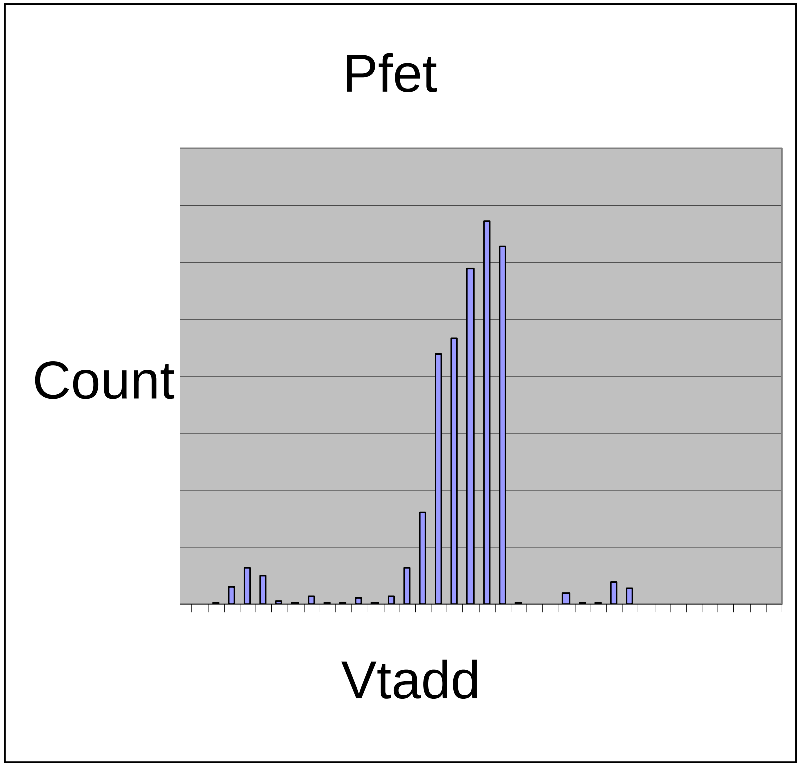


Treating arbitriary functional forms is needed to correctly capture the many phenomenon that impact CLY

$$VtAdd = f(W, Dis)$$

$$VtAdd = a_o + a_1 e^{w} + a_2 w e^{w} + a_3 e^{Dis} + a_4 Dis e^{Dis}$$

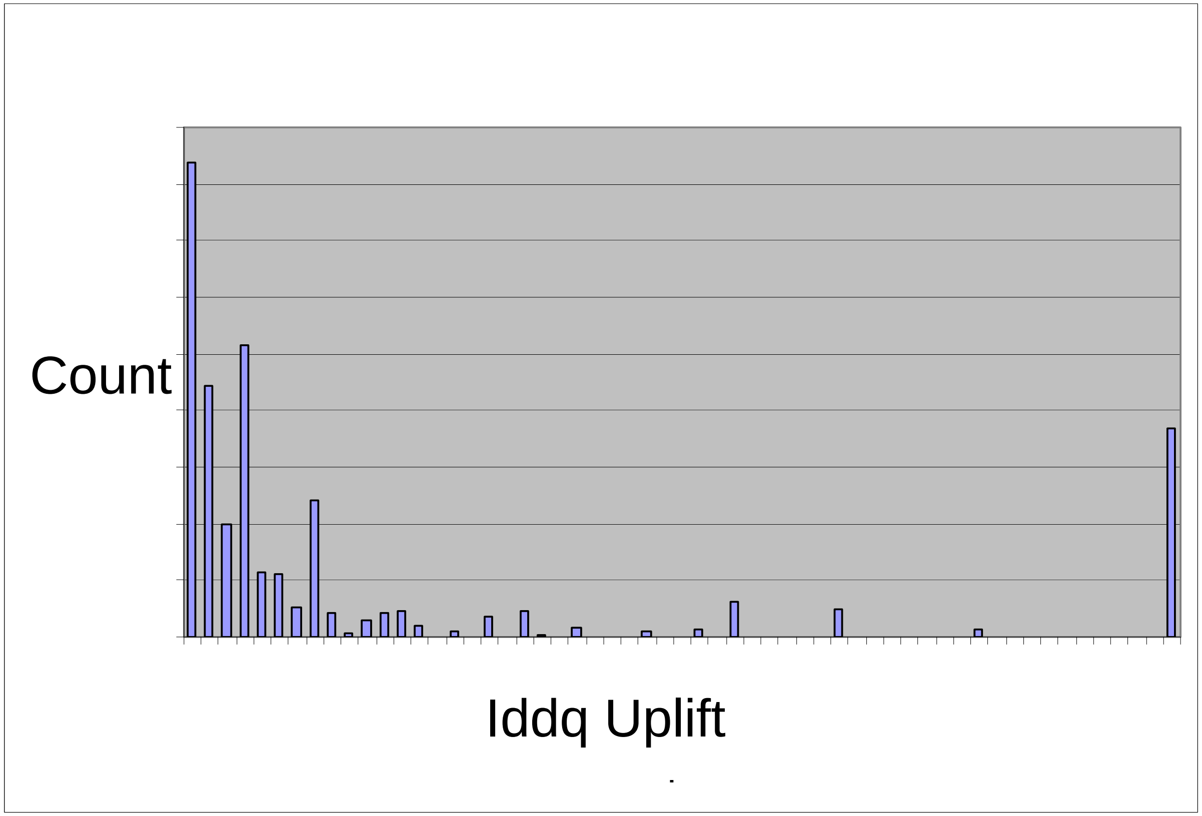


## Treating non-Gaussian distributions is a requirement. Foundry Pleak predictions require each gate to be analyzed individually.

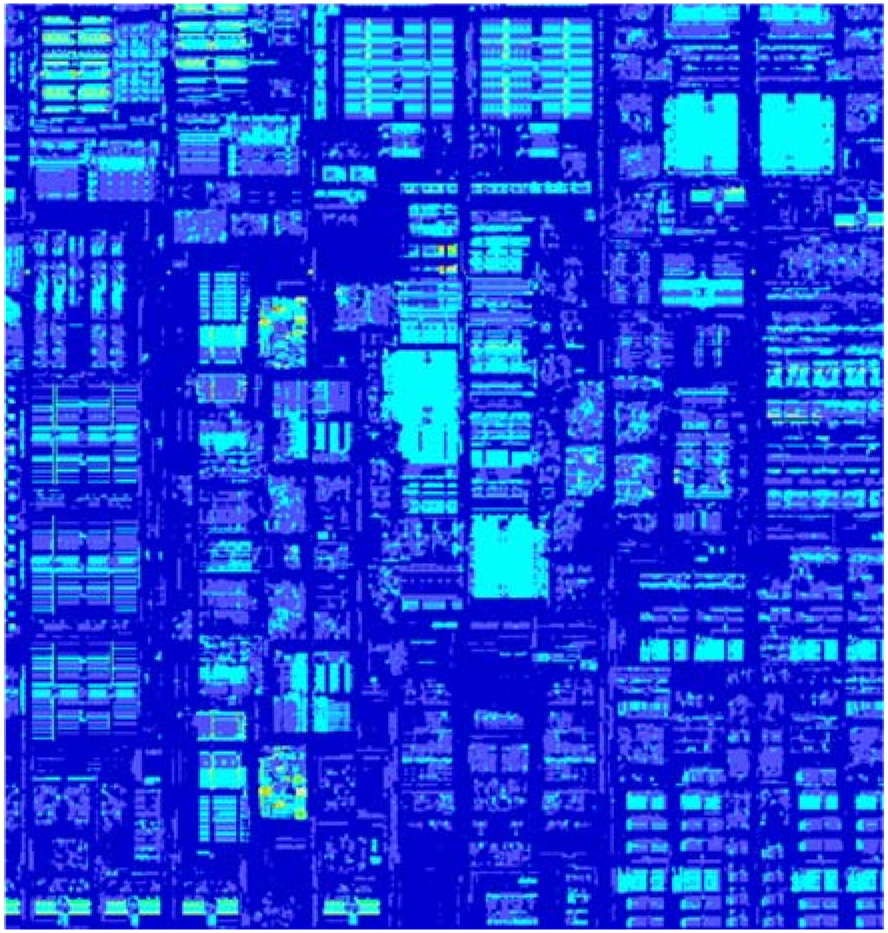
$$N_{NCE} = e^{\left(a + \frac{b}{\cosh(w) - 1}\right)}$$

| Device Type | a | b |
|---|---|---|
| Rvt Nfet | a1 | b1 |
| Hvt Nfet | a2 | b2 |
| iLvt Nfet | a3 | b3 |
| Rvt Pfet | a4 | b4 |
| Hvt Pfet | a5 | b5 |
| iLvt Pfet | a6 | b6 |



# Full Circle

- **Equation DRC provides for CLY prediction**
  - GateSpace stats
  - GateWidth Stats
  - GateLeff stats
  - SA/SB stats
  - NWscattering stats
  - CR stats
  - Device type and count numbers
  - Gate Area stats
  - Calculations of Iddq nominal
    - With NW proximity
    - With NCE
    - With CR, and pitch
    - By cell
    - Full chip
    - By region

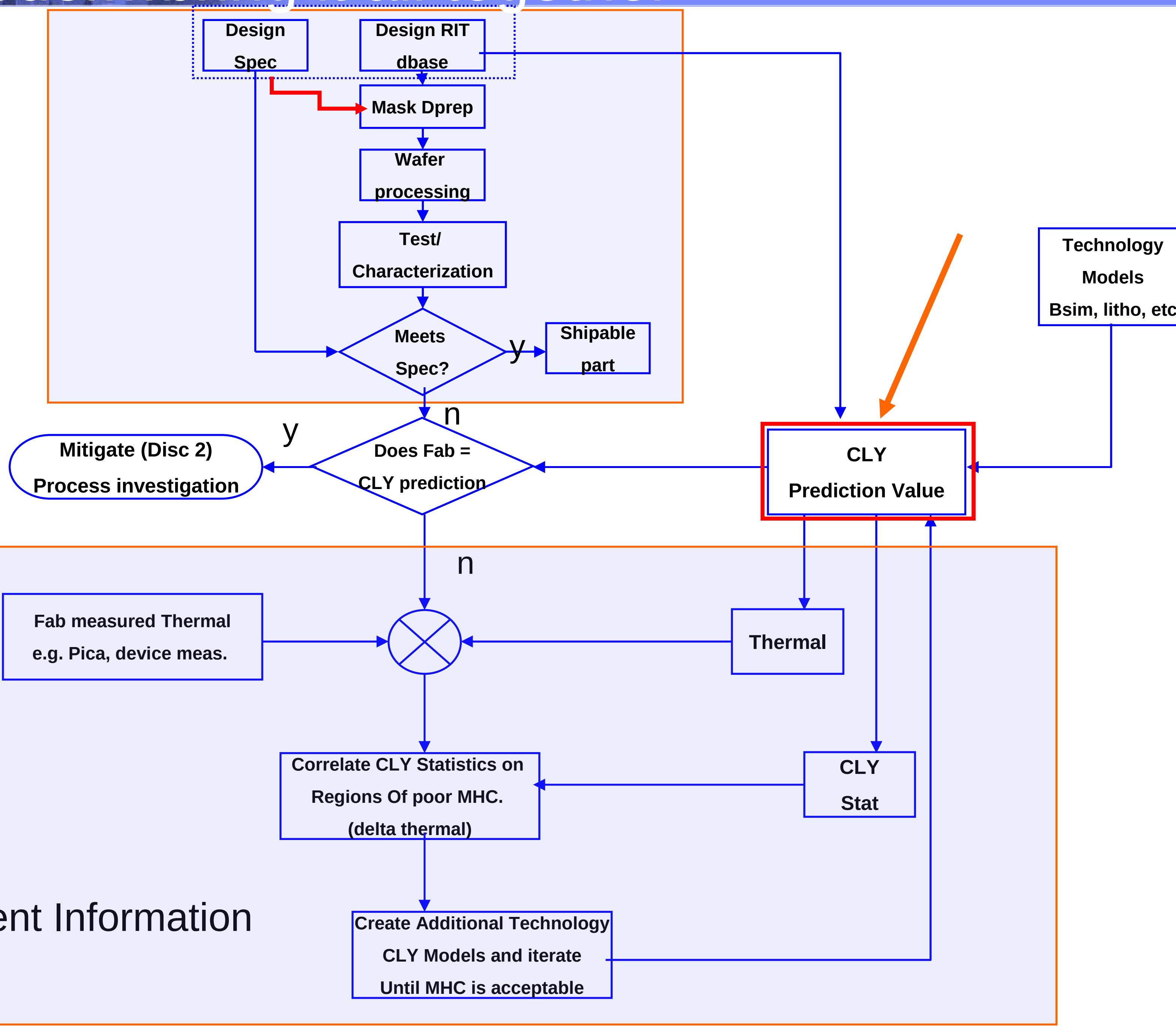


$$IdsatIndex = \Sigma \alpha n \Delta P\mathrm{n}$$

$$IddqIndex = \Sigma \beta n \Delta P\mathrm{n}$$

Full Chip prediction
maps for all current flow phenom.

# CLY – Model…bring it all together



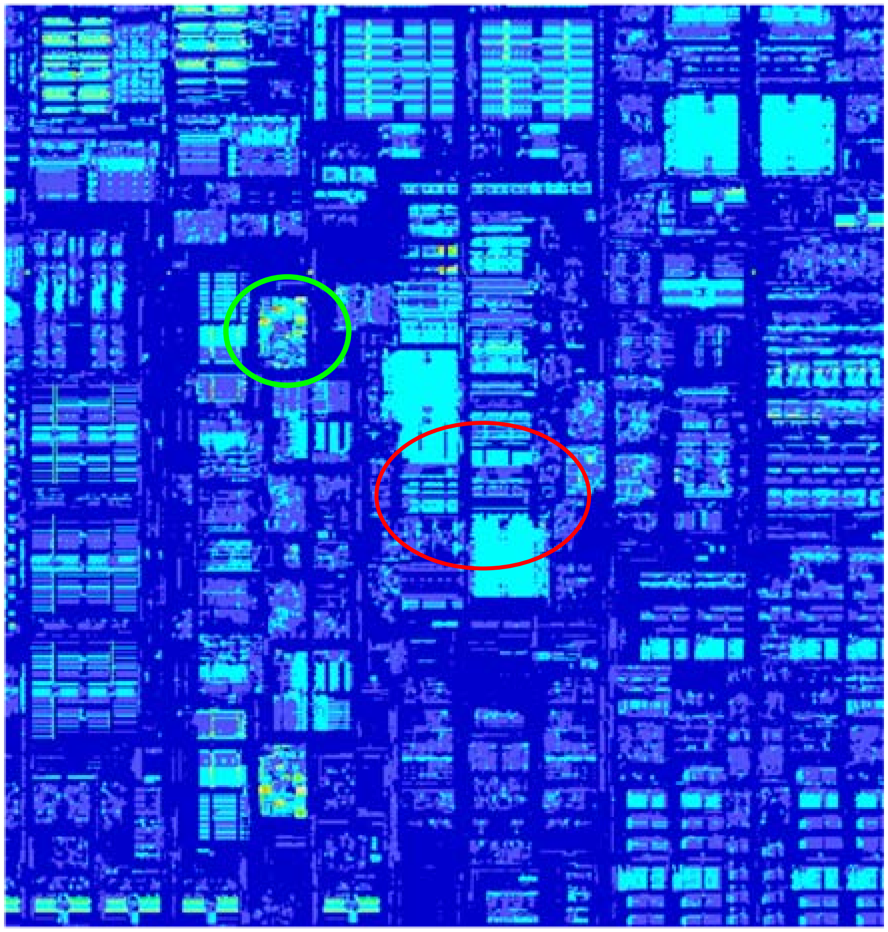

Design Intent Information

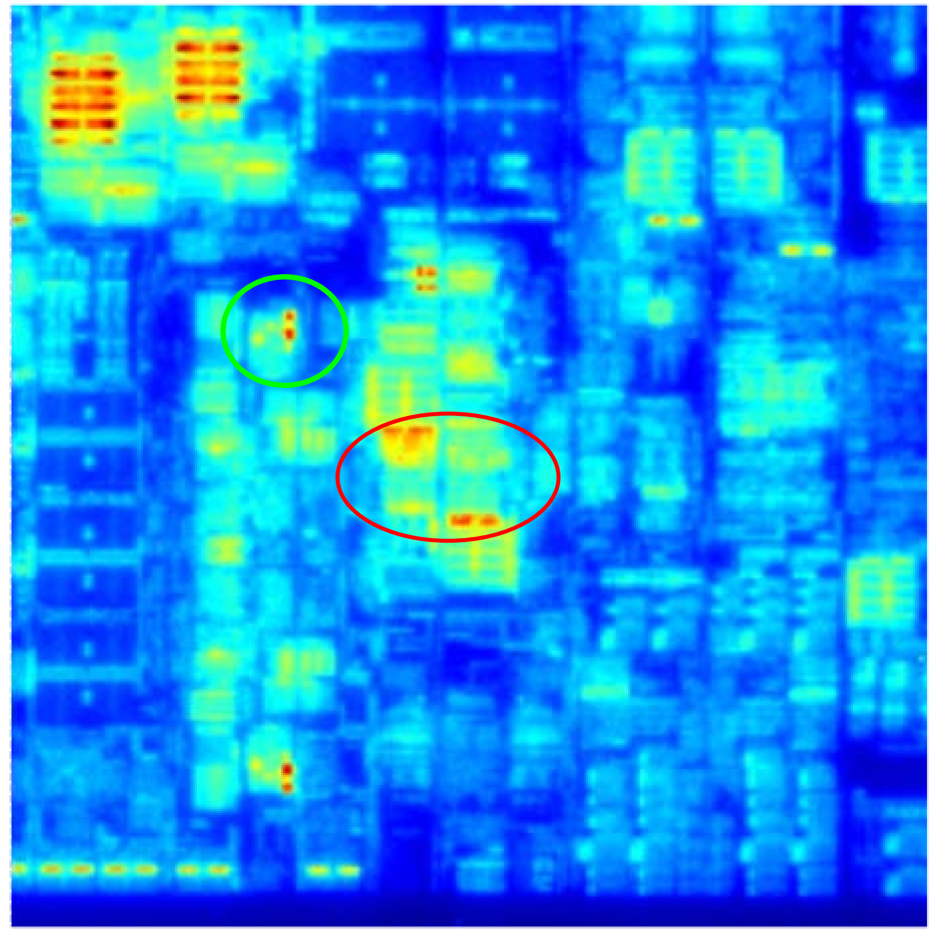


United States Patent Application 20090106714

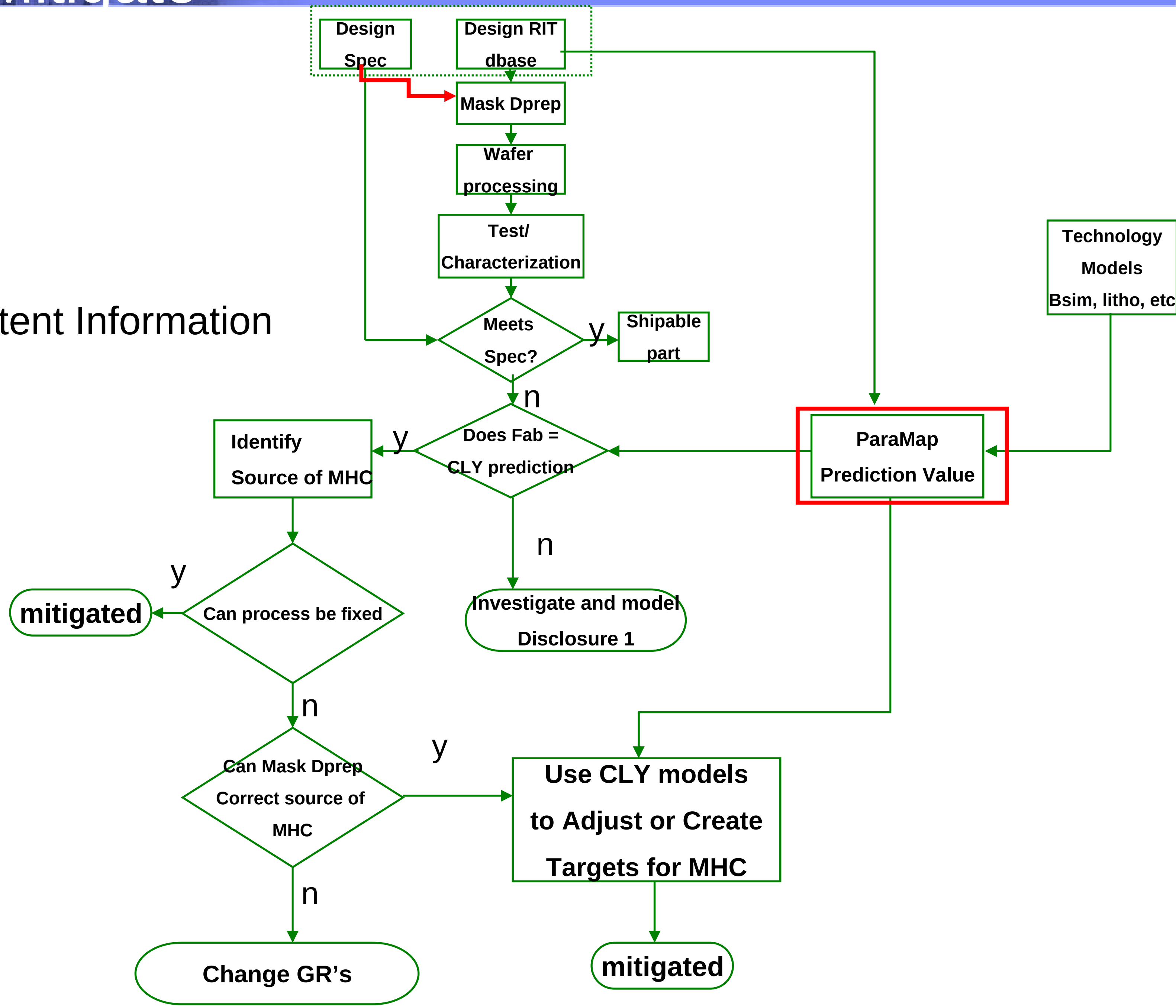
# Post Processing yield mitigation

Thermal prediction and physical Emission picture.
Image Delta finds regions of increased deviation from Model (MHC)





Design Intent Information






United States Patent Application 20090106714

# Conclusions

- **Circuit limited yield poses new challenges to manufacturing and design teams for sub-65nm technology.**
- **CLY can be mitigated through the 3 step process**
  – Measure
  – Model
  – Mitigate
- **EqDRC has proven itself irreplaceable**
  – When arbitrary model forms are needed.
  – In appropriately treating and balancing multiple sources of variation, and/or multiple phenomenon.