



RESEARCH BRIEFS

Mentor's Design to Silicon Division : Next Generation 45nm Platform

Mentor Graphics, launched its coordinated software/hardware platform effort (November 29, 2006) between Mercury Computer Systems and IBM Corporation. Mentor noted that its next generation Calibre nmOPC, (optical proximity correction) tool will be migrated to Mercury Computer System's Cell BE (Broadband Engine) cluster. As part of the announcement, Mentor's Calibre nmOPC tool stated that it has development support coming from Intel and IBM, and 4 other IC manufacturers. Mentor and Mercury will jointly develop this new EDA platform. The Cell BE (Broadband Engine) processor from IBM, is based on a development collaboration between IBM-Sony-Toshiba, established in 2000. The Cell BE was originally produced for the Sony PS3 consumer products. Mercury Computer Systems is now designing it into medical imaging, aerospace, video processing and seismic processing applications.

Mercury's design and manufacturing strengths are at the hardware system and sub-system assembly level. Mercury also brings a history of ASIC component and embedded coprocessor design capability that is used in communications, medical, compute and military system applications. IBM's Cell BE technology supports the future alliance roadmap between Mentor and Mercury. IBM's Cell BE 2006 roadmap is a 90nm process based on SOI (Silicon on Insulator). The 65nm SOI based product will be introduced in 2007, followed by an enhanced 65nm processor in 2008. The next generation 45nm SOI 1TFlop design is forecasted for introduction in 2010. The existing Cell BE is a nine core chip with 241 million transistors, at 235 MM2, using Rambus DRAM chips.

According to Mentor, Mercury and IBM benefits to users include:

- Lower hardware cost
- Lower power cost
- Lower cooling cost
- Lower capital equipment investment
- Quicker turnaround time
- Improved application performance

The combined efforts of Mentor-Mercury-IBM are to reduce current complexity and design costs of 90nm and 65nm designs at the chip and system level. The overall roadmap for future developments and tool solutions is to pave the way for design challenges that need to be addressed for 45nm developments, expected to come on-line in 2007 and 2008. The overall benefits from this coordinated effort include improvements in yield and final chip performance, power reduction, chip size and board size/space reductions, thereby reducing the overall cost of ownership.

Mentor's announcement sends a clear signal to the competition that they are the one to beat. Mentor continues to lead the market in their understanding of the entire DFM challenge, by introducing the tools needed to surmount that challenge. Their competition, both large and small, provides the point tool approach to the solution. Mentor is doing their best to supply the whole solution.

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