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Lithography: The Integration of TCAD and EDA

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At a Glance

Particularly with the growth of the fabless/foundry model, simulation tools embedded into EDA tools will become more prevalent. The overall value of incorporating detailed simulation within the EDA tools themselves has been clearly demonstrated for lithography.

At the time when Gordon Moore made his original observations later to become known as Moore's Law, process development was a solidly experimental discipline. Layouts were made by cutting rubylith by hand, and photo reduced to create masters, which in turn were used to make the masks that stamped out the ICs through a contact printing process. Process corrections were done by hand, and biasing was a global process tied to over- or under-developing.

The compelling economics of Moore's Law, however, with its virtuous circle of smaller feature dimensions, higher feature density, and exponentially decreasing cost per transistor, meant that the size of electronic devices would inexorably shrink, and their number would exponentially grow. To simply manage the design challenges involved, the electronic design automation (EDA) software industry emerged, using newly developed computers to design newer and faster generations of computers.

Process development, however, was still an empirical domain. The typical lithography engineer had a background in chemistry, not computer science or simulation. The emergence of high-precision electron-beam lithography tools to make masks provided a nearly perfect original pattern to be used for subsequent projection printing, and the ability for imaging processes to faithfully reproduce those patterns was a matter of managing the resist exposure and development parameters.

Process modeling did make some steps forward. Lithography modeling received a great deal of attention. The creation of the Dill model for process development in the 1970s provided a set of parameters to be used for comparing and better understanding resist kinetics, and this became used for the formulation of ever more specialized

photoresists. Optical models of the imaging process were pursued at several academic institutions, with an eye on the time that current procedures might break down. Programs like SAMPLE and SPLAT were developed at UC Berkeley, while PROLITH emerged as a combined imaging and process simulator.

The emergence of modeling programs for other aspects of device fabrication created a small software industry that became known as technology computer-aided design (TCAD). The dominant player in this market was the company Technology Modeling Associates (TMA), founded out of Stanford University. TCAD groups were formed at most major semiconductor manufacturers, creating a healthy, if small, market for these simulation tools.

The appeal of these initial modeling programs was more that they allowed engineers to make "virtual" experiments without taking the time or wasting the silicon for the initial trials. Once optimal parameter settings were suggested by the simulation results, however, the final experiments were still run on the fab. The approximations in the modeling programs allowed these tools to identify trends and guide experimental design, but the trust in the calibration of their final results was simply not there. However, with wafer sizes moving from 3 to 6 and then to 8 inches in diameter, replacing even some of the experimental protocol by simulation could have significant cost savings, and certainly enough to pay for the TCAD tools several times over.

In the 1990s, a sea change began to happen. The number of transistors in an IC design grew so large that the only practical approach to design was by using automated software tools. The assumptions underlying those tools became masked as the user grew ever more distant from the underlying devices and processes used to make those ICs. The need for better models and better calibrations began to grow.

As computing power became more inexpensive, better models could be developed without the limiting approximations previously required to achieve closure. Lithography modeling was an early area where modeling needed to be revised. In the mid-1990s, the progression of smaller feature sizes under Moore’s Law approached and eventually crossed the dimensions of the wavelength used for lithography. Since the 180 nm technology node, imaging features smaller than a wavelength would now be routine for all critical layers.

In subwavelength imaging, process distortions are routine, and correction algorithms must be run on layouts to compensate for them. This process is generally called optical proximity correction (OPC). With the subwavelength era, OPC became mandatory, and modeling tools that routinely integrated lithography simulation became integrated into conventional EDA software tools.

This created a very powerful combination. No longer was the simulation being carried out offline in a separate TCAD group, only on abstract designs and test patterns, but now every polygon of every layer was automatically evaluated for process failure. Every point of failure could then be corrected, or flagged for redesign. The ability for the hierarchical engines of verification products to maintain layout hierarchy while still addressing these simulation challenges created exceptionally powerful tools that changed the product world of layout verification, formerly a sleepy world of simple design rule checking (DRC), to a dynamic process modeling suite of operations, checking a circuit layout for a variety of faults before final shipment to maskmaking and wafer processing.

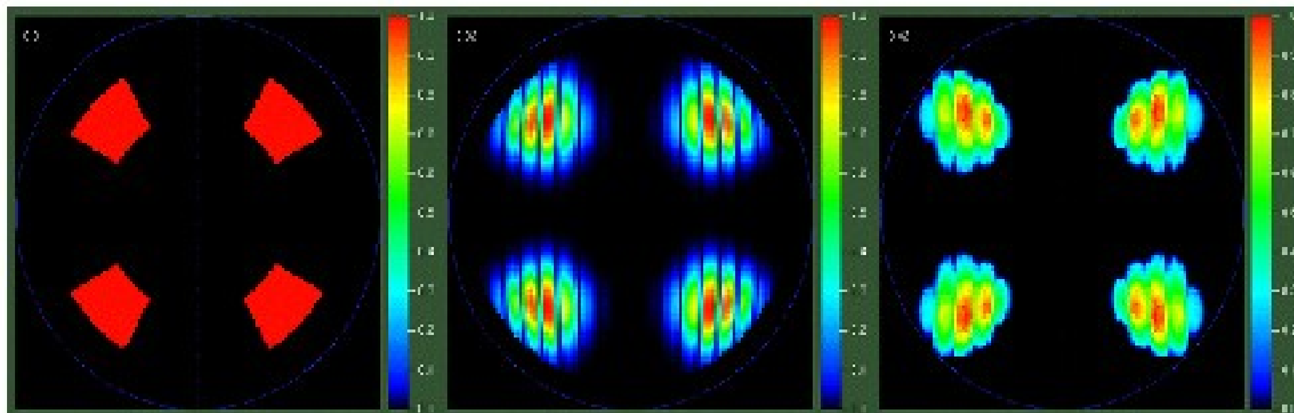
The ability for these new, powerful modeling tools to handle large designs is impressive. However, the

weak link in this chain, as in the older TCAD days, is calibration. A model will only predict as well as the calibration information that is given it, and here the procedural ability of fabs has not kept up with their computational ability.

One example of some of the subtleties that are now being encountered for the 90 nm node has been recently reported by Yuri Granik and Nick Cobb.[1] Here, the model for the through-pitch behavior for 180 nm lines was found to deviate from the measured behavior by >15 nm for pitches between 600 and 800 nm. Although 15 nm may sound like a small number, it consumes the entire error budget allowed for a 90 nm process, and is clearly unacceptable.

In the past, the model would be blamed as simply inaccurate, and a better model sought. With the current trust in the expanded models used in commercial OPC software, the assumptions behind the model now warranted an investigation.

In this case, Quasar illumination had been used in the exposing stepper, and the nominal map of a Quasar illumination source is as shown in Figure 1a. However, this clean illumination pattern is not what emerges from any real illumination system. Replacing the illumination pattern in the simulator with a pattern more typical of the output of real illumination systems (Fig. 1b) produced simulation results that agreed quite well with the measured values — with no change in the underlying optical simulation models themselves. Subsequent measurement of the actual illumination (Fig. 1c) found a good match to the revised pattern. In this case, the simulation engine itself was accurate, but the performance was only as good as the input to the model.



1. These maps show an idealized illumination source map for Quasar illumination (a); a prediction of a more realistic source map from the properties of the illuminator (b); and actual measurement of the illumination source (c).

In the case of illumination, generation of accurate maps of source illumination
are possible, and tools are commercially available should they be desired. However, for other input parameters challenging lithographic modeling, such as the availability of accurate lens aberration parameters, the situation is less clear. The incorporation of subtle effects, such as long-range effects, including flare and those caused by etch microloading, are also becoming significant. And a fundamental problem with input calibration remains unaddressed: line-edge roughness and metrology error.

Currently, most wafers are measured using commercial SEMs. These are generally able to make measurements with nanometer-level accuracy. However, repeated exposure of resist to electron beams can both charge the resist and cause real erosion of the physical structures. Both will cause real distortions in the linewidths measured, often by several nanometers. Unless care is taken to ensure that the metrology protocol is exactly the same for every measurement, both during calibration and after measuring final results, measurement uncertainly will increase.

The definition of a line edge itself is also under some question. Common CD-SEMs will generate their measurements of a linewidth by averaging over several locations of a line. For photoresists, the molecular structure of the material will lead to a certain "lumpiness" in the edge of the resist. It is therefore difficult to accurately define what exactly the "linewidth" of such a lumpy structure really is. However, simulation engines typically assume perfectly uniform resists, without considering molecular structure. Some simulations of this granularity have been done, notably at the University of Wisconsin. The incorporation of these more accurate molecular models into simulation engines may be required if subnanometer accuracy is truly desired.

So far, only changes needed in lithographic modeling have been discussed. There are other areas in which the modeling assumptions must be revisited as well. The realization that parasitic inductance will have to join parasitic capacitance in extraction evaluations also will lead to a revision of the models used in those products. In this area, the challenges of calibration and accuracy will also be significant, and new protocols to metrology that best capture the subtleties of these effects will emerge to dominate these markets.

In the past, Jerry Saunders, CEO of AMD, could boast that "Real men have fabs," and that simulation and virtual processing were adjuncts to the business of making ICs. Now, with an evolution of more and more ICs to the fabless/foundry business model, the adoption of "virtual fabs" in the form of simulation tools embedded into EDA tools by more and more companies will become a reality. The overall value of incorporating detailed simulation within the EDA tools themselves has been clearly demonstrated for lithography, and is expected to continue in other areas of process simulation as well. As Moore's Law continues to drive the cost of computing down and the need for more subtle models increases, the integration of what was process and manufacturing models into EDA should be expected to continue.

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