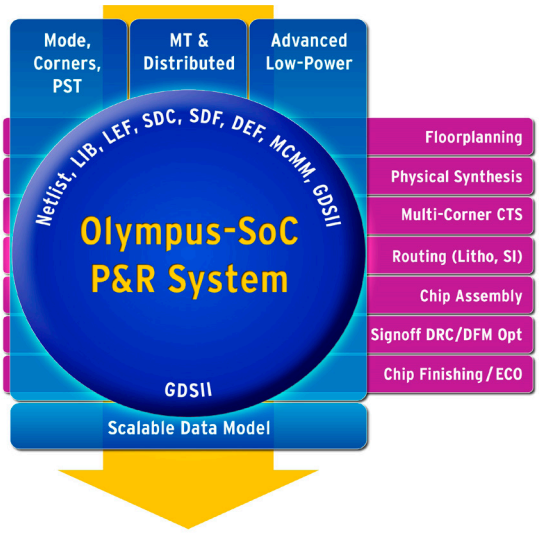
Olympus-SoC



Olympus-SoC offers powerful Multi-Corner–Multi-Mode timing for variability and manufacturing optimization in all physical design steps.

Solving Advanced Node Design Challenges

The Olympus-SoC™ Netlist-to-GDSII system comprehensively addresses the performance, capacity, time-to-market, and variability challenges encountered at the leading-edge process nodes. It has the highest capacity architecture, a native sign-off quality timer with patented virtual timing graph technology, and best-in-class physical implementation engines.

With Olympus-SoC, you can account for design, process and lithography variation throughout the IC design flow. Integral to Olympus-SoC is the next-generation routing engine, which embeds variation-aware timing, optimization and litho-modeling to address OPC and RET effects early in the design cycle and ensure faster timing closure for complex process rules at advanced design nodes. Olympus-SoC was architected specifically to address three critical design challenges at advanced process nodes: manufacturability, variation-based timing closure, and extremely large design data sets.

Variation-Based Timing Closure

Leading-edge designs need to be analyzed and optimized for various design contexts and timing variations due to device/interconnect scaling. Using approximations, like constraint merging or adding margins, results in loss of accuracy that impacts design yield, timing closure, and time-to-market.

You can avoid unpredictability in sign-off ECO loops, eliminate performance-killing pessimism, and speed the time to tapeout when you consider all the scenarios concurrently, from floorplanning to GDSII-out. Olympus-SoC's patented and tape-out proven Multi-Corner–Multi-Mode (MCMM) architecture drives the router and optimization engines to automatically achieve timing, power, signal integrity, and manufacturability closure across all modes and corners concurrently.

Benefits

- **Boost IC performance** with advanced multi-corner, multi-mode optimization
- **Improve yield** with DFM-aware routing to address lithography issues in a timing context during implementation
- **Speed time-to-market** with fewer design iterations, scalable multi-threading, and sign-off quality closure
- **Reduce costs** through high yields and fast time-to-market

Major Product Features

- Patented MCMM optimization during all design steps
- Fast routing with full rule support for the most advanced nodes
- Sign-off quality timing analysis and optimization
- Extremely fast and accurate, on-the-fly parasitic extraction
- Floorplanning, rapid design feasibility and constraint debugging
- Best-in-class, CTS-aware standard cell and macro placement
- Industry's first MCMM CTS for robust, low-power clock trees
- MCMM SI to concurrently compute delay shift and glitch for any number of mode/corner scenarios in a single pass
- Advanced physical synthesis with built-in OCV and CPPR
- Handles multi-million gate designs hierarchical or flat with faster runtimes

MCMM Clock Tree Synthesis

Variations in resistance can cause large deviations in clock skew across different process corners. Olympus-SoC addresses this problem by using advanced MCMM clock tree synthesis technology, with automatic OCV, to simultaneously optimize skews across all process corners concurrently. This results in robust, low-power clock trees that are resilient to process variations and show significant improvement in the number of buffers, total area, timing and power.

MCMM Signal Integrity Closure

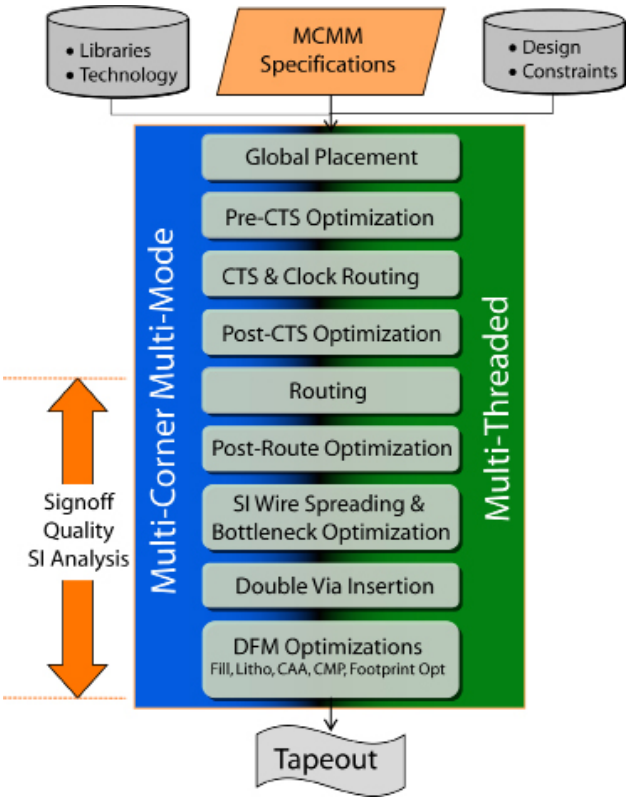
The MCMM signal integrity (SI) prevention and repair flow ensures that your design meets SI constraints across all your design modes and corners. Olympus-SoC uses on-the-fly, multi-CPU extraction to keep the database constantly in sync with changes as they happen.

Extraction is also incremental, so only changed wires are considered. Fast extraction and the MCMM timing engine accurately analyze potential SI violations, driving the router to use a variety of techniques to minimize or eliminate crosstalk, delta delay, delta slew, and glitch violations.

Routing for Manufacturability and Yield

At 65 nm and 45 nm process node manufacturing, there is increasing distortion between the printed patterns and the intended structures in the layout database. These distortions cause faults such as bridging, pinching and via failures. Olympus-SoC uses a multi-CPU, DFM-driven routing engine, which was built from the ground-up to address complex DRC rules and lithography errors.

By using dynamically updated information from the embedded shape-based DRC engine, Olympus-SoC assumes the "as manufactured" shapes and geometries for both devices and interconnects during routing. With additional layout enhancing techniques such as wire spreading, redundant via insertion, jog-widening, and timing-driven metal fill, Olympus-SoC produces inherently lithography-friendly designs.



Every step in the Olympus-SoC Netlist-to-GDSII system is MCMM and multi-threaded for unparalleled design quality and the shortest turn-around-time.

Low-Power Support

In addition to performing concurrent timing and leakage optimization, Olympus-SoC supports a variety of low-power styles, such as multi-voltage, multi-threshold designs. Olympus-SoC delivers the lowest power consumption and fastest time to design closure with powerful MCMM leakage and dynamic power analysis and optimization.

High-Capacity Architecture

The ever-growing design sizes can overwhelm older design tools, but Olympus-SoC's very high capacity, 100 million gates or more, frees designers to implement their designs flat or hierarchical. The ultra-compact architecture is flexible and open for easy integration into existing design flows.

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