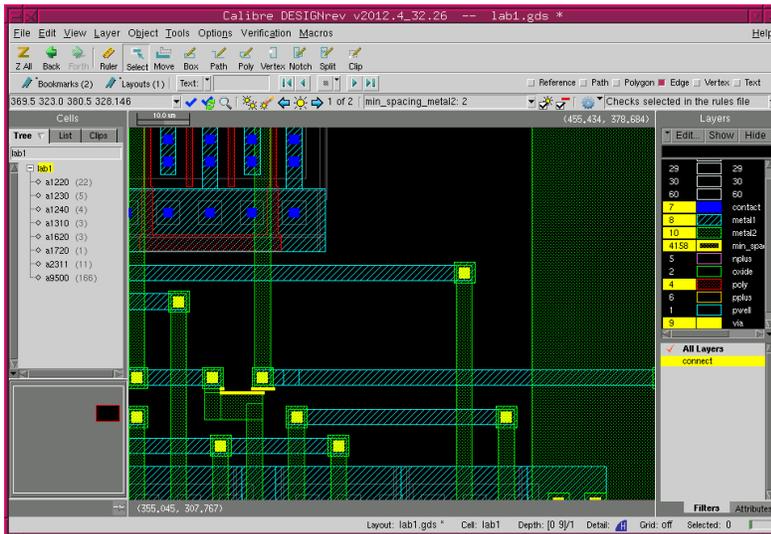


# Fast, Flexible, and Robust Chip Finishing Calibre DESIGNrev

Physical Verification

D A T A S H E E T



Calibre DESIGNrev's robust and flexible chip finishing and review capabilities let users speed through full-chip design completions and tape-outs for even the largest GDSII/OASIS files with Calibre confidence.

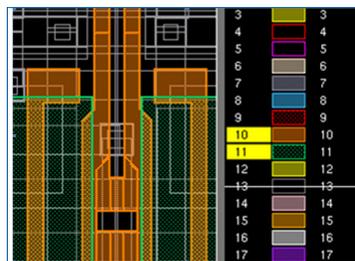
## Fast and Flexible Chip Finishing Platform

Calibre® DESIGNrev loads and displays the largest layouts on a typical engineering workstation in seconds. The incremental loading capability provides a scalable solution that is less dependent on I/O, and more efficient for multi-site collaboration. Calibre DESIGNrev also provides an extensive set of debugging features, including net extraction and visualization, overlay, and editing. Users can directly manipulate native GDSII/OASIS database objects such as cells, instances, polygons, edges and text. Calibre DESIGNrev's net extraction and editing features provides easier setup and migration between process nodes for CAD engineers, as well as accurate, easy-to-use net visualization. Its extensive capabilities, combined with its user-friendly design, make Calibre DESIGNrev the high-performance tool for fast, accurate, and efficient chip tapeout preparation.

## Express Drawing Engine

The express drawing engine provides fast and easy navigation, enabling rapid viewing/zooming/panning of layouts, as well as layer visibility.

- Instant pan and zoom
- Emphasize selected layers while other chip structures remain visible



Emphasize selected layer for point inspection.

## Lightning-Fast Chip Assembly

Calibre DESIGNrev effectively manages the most challenging chip assemblies with its ability to process massive databases in very short runtimes while using a small memory footprint.

## BENEFITS:

- Complete chip finishing platform
- Lightning-fast and easily customizable chip assembly process
- Accurate, fast debugging for the most complex designs
- Tight integration with the Calibre platform provides a full range of signoff-quality verification features
- Rapid layout review handles the largest files with ease
- Fast and easy navigation for viewing/zooming/panning layouts

## FEATURES:

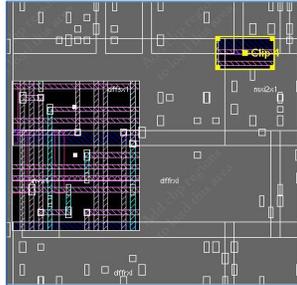
- Express drawing engine
- Extremely fast database merge with minimal memory
- Loads massive files in seconds on typical workstations
- Fast, flexible overlay and compare functionality
- Fast layout viewer integrated with lithography simulators and editors supports GDSII and fracture formats
- Full range of advanced debugging capabilities
- Extensive batch and interactive editing
- Calibre WORKbench TCL/TK API
- Support for GDSII, OASIS and Gzipped layouts
- Fast database format converter and optimizer
- Direct read OpenAccess, Milkyway, and LEF/DEF
- Realtime signoff DRC with Calibre RealTime integration

- Merge 10Gb of data in as little as 10 minutes
- Supports GDSII, OASIS, and Gzipped layouts
- Agile modes enable one-pass merging for even the most complicated tasks

## Unlimited Capacity with Incremental Loading

Calibre DESIGNrev's incremental loading capabilities ensure the most efficient and effective use of resources.

- Unlimited capacity allows users to load multi-Tb layouts on typical engineering workstation in seconds
- Shared cache file efficient for multi-site collaboration
- Less dependent on I/O because less data is transmitted
- Load, review and manage polygons and hotspots as needed



*Clip layout to load, view, and save hotspots as needed.*

## Flexible Chip Review with Overlay

Calibre DESIGNrev allows users to place two or more layouts in one canvas, making it easy to perform a variety of chip finishing functions:

- Compare layouts visually or with XOR results
- Complete visual chip assembly with block-level GDS files
- Verify IP block in full-chip context
- Measure alignment of MDP files
- Shift, magnify, rotate and mirror a single layout

## Superior Layout Manipulation Debugging Capability

Calibre DESIGNrev provides a full range of advanced debugging capabilities. The extensive debugging feature set includes:

- Layer control and filtering for better visibility of context
- Net extraction and visualization
- Extraction of entire net or nets in selected region
- Point-to-point shortest path tracing
- Interactive and batch editing of native GDSII/OASIS database objects (e.g., cells, instances, polygons, edges, text)

## Calibre WORKbench TCL/TK API extension

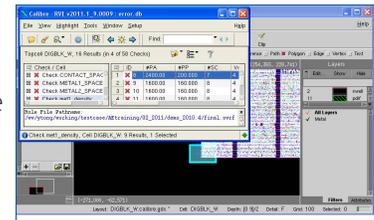
With its support of open standard TCL/TK, Calibre DESIGNrev makes it easy for users to customize and simplify their chip finishing process:

- Fast/flexible batch processing for GDSII/OASIS data with scripting
- API to call commonly used Calibre DESIGNrev functions

## Tight Calibre Integration

Calibre DESIGNrev is part of the Calibre nm Platform, the industry's leading physical verification platform, providing users a full range of signoff-quality verification features:

- Calibre RVE – quick error identification and cross-probing
- Calibre Interactive – customizable invocation for Calibre tools
- Calibre RealTime - invoke realtime signoff DRC checks during design modification (requires Calibre RealTime license)



*Navigate through layouts quickly and easily.*

- Verify and re-verify entire design, or just the portion being modified with incremental DRC
- Calibre's best-in-class performance, accuracy and reliability delivers Calibre sign-off quality and confidence

**For the latest product information, call us or visit: [www.mentor.com](http://www.mentor.com)**

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