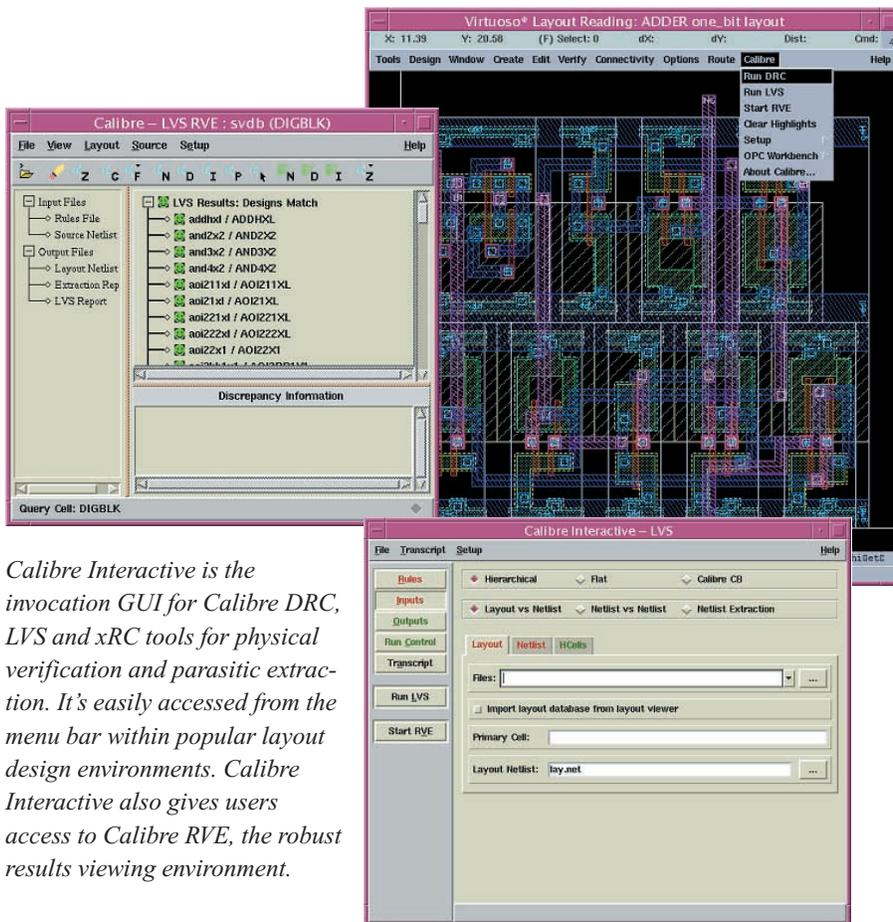


# Calibre Interactive



*Calibre Interactive is the invocation GUI for Calibre DRC, LVS and xRC tools for physical verification and parasitic extraction. It's easily accessed from the menu bar within popular layout design environments. Calibre Interactive also gives users access to Calibre RVE, the robust results viewing environment.*

## Calibre Interactive offers push button access to Calibre physical verification and parasitic extraction tools.

Calibre Interactive™ provides users with fast and easy access to the Calibre® tool suite, enabling designers to perform physical verification and parasitic extraction from within their familiar integrated circuit design environment. Designers using Cadence Design Systems® Virtuoso, Synopsys® Apollo/Astro, or Mentor Graphics® IC Station can adopt a single verification and extraction solution for their entire physical design flow, regardless of design style or methodology. Calibre offers a robust design-to-silicon tool suite for designers working with cell/block, full chip, analog, digital, analog/mixed signal, or systems-on-chip designs.

## Key Product Benefits

- **Tightly integrated with popular design tools.** Calibre Interactive can be launched from the command line or tool bar within Cadence Design Systems Virtuoso, Synopsys Apollo/Astro and Mentor Graphics IC Station.
- **Customizable interface.** Provides users with internal mechanisms that allow CAD teams to customize the design environment for their users.
- **Provides a single interface for physical verification and parasitic extraction.** Calibre Interactive provides design teams with a single portal for performing DRC, LVS and parasitic extraction on supported platforms.
- **Eliminates costly maintenance associated with supporting multiple verification tools.** Training, support, documentation, rules file support, installation and upkeep is simplified to a single tool suite.
- **“Launch and load” with Calibre RVE.** Automatically launches Calibre’s Results Viewing Environment when verification run is complete and loads results.

## Single Verification Flow Solution

Because Calibre is design style independent, designers can use Calibre as a single physical verification and parasitic extraction flow for designs containing analog, digital, mixed signal or RF components. A single tool for designs digital, mixed signal or RF components. A single tool for physical verification in cell/block and full-chip eliminates the discrepancies caused by out-of-sync verification rules. It also eliminates maintenance associated with supporting multiple verification flows.

## Integrated Within Supported Layout Environments

Designers can invoke Calibre Interactive within popular design environments such as Cadence Virtuoso, Synopsys Apollo/Astro, and Mentor Graphics IC Station. Designers can perform verification or extraction from within the design environment using the same rule file for cell/block or full chip.

## Customized Runset Options

Runsets are templates created by CAD teams and used in Calibre Interactive to ensure designers have access to correct rule files, run directories and other required settings. Using runsets eliminates common issues encountered when launching physical verification or parasitic extraction.

## Triggers

Triggers are a very powerful tool for customized integration. CAD teams can use pre- and post-execution triggers to run proprietary scripts before or after Calibre runs.

## Customized GUI Options

CAD teams can define a customization file that generates a customized GUI.

This GUI gives users control over the Calibre execution. A customized file will open a customized GUI prior to Calibre Interactive. This GUI contains radio buttons and cyclical fields that users can select. CAD teams use customized GUIs to specify statements in the Calibre rules file, such as Define Select Check and variable statements.

## Calibre Interactive and DRC

Designers can specify and run individual or groups of checks from Calibre Interactive. Designers can also perform Area DRC on a select area of a large design to reduce translation time and to cut verification cycle time during debugging.

## Calibre Interactive and LVS

Calibre LVS provides layer options for shorts isolation. It will automatically translate layout data to GDSII and schematics to netlist when invoked from supported tools.

## Calibre Interactive and Calibre xRC

Users can control parasitic extraction variables in Calibre xRC and specify the type of parasitics to extract, whether C, RC, or RCC. Users can also specify a run on a specified net. Designers have a

choice of an output netlist to H-SPICE, DSPF or Calibre View, which can be used to generate an extracted schematic view inside the Cadence DFII database. Designs referencing this view in their testbench can run simulation and see the resulting parasitic effects on their design.

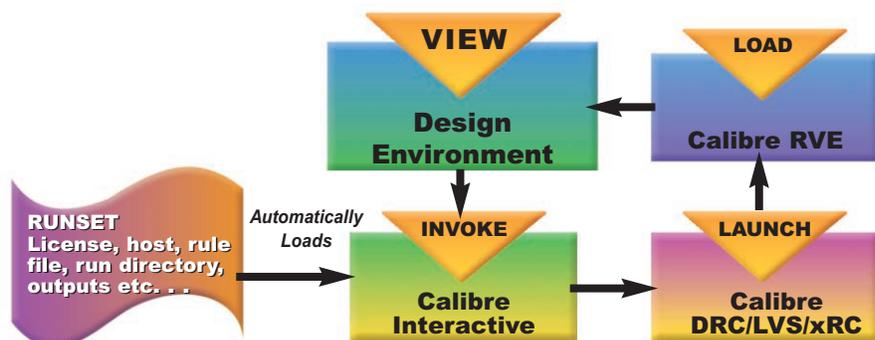
## Calibre Interactive and RVE

Calibre's robust results viewing environment offers visualization for debugging of Calibre results. The tool highlights DRC errors, and recognizes nets, devices and parasitic data to native layout and schematic windows. Calibre RVE also highlights to the source and extracted netlists, which gives designers more information for debugging circuits. Complex nets can be traced with the SPICE netlist browser.

## Calibre Widely Supported in Industry

Calibre is the standard for accuracy at a majority of semiconductor foundries, including Chartered, IBM, TSMC, UMC, Jazz and many more. Designers can take advantage of the large number of fully qualified Calibre rule files supported by the foundries as the golden sign-off standard.

## Runsets in a Calibre Flow



Visit [www.mentor.com/dsm](http://www.mentor.com/dsm) for the latest product news and technical publications.

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