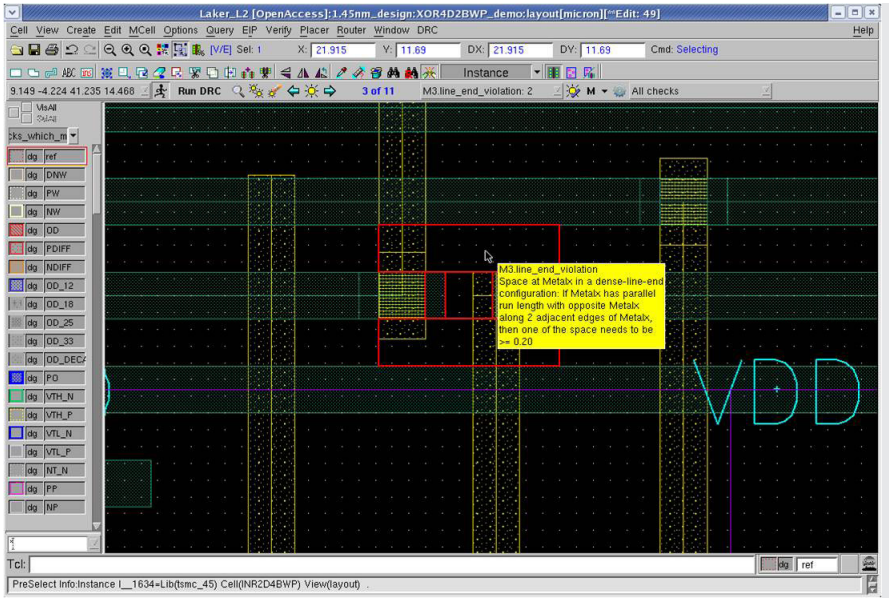
Verification

Calibre RealTime

Calibre signoff-quality verification on demand in custom/AMS design flows

D A T A S H E E T



The Calibre RealTime platform completely changes the traditional layout-verification-simulation loop by bringing signoff-quality verification into the design creation process.

Signoff-Quality DRC during Design

Calibre® RealTime enables in-design signoff-quality Calibre design rule checking (DRC) for custom and analog/mixed-signal design flows, improving both design speed and the quality of results by providing immediate feedback on design rule violations and recommended rule compliance. With this information readily available during layout, designers can optimize designs for increased performance without incurring numerous time-consuming design-verification iterations.

By providing the same automated check capabilities available to digital design checking, Calibre RealTime makes it easier for custom IC designers to produce high-quality designs while still meeting production schedules. Now, no matter how many drawn layers a design contains, or how many checks there are per layer, or even how complex those checks are, design groups working at the most advanced nodes can get to DRC-clean quickly and with Calibre confidence.

When integrated into a custom IC design and layout system, Calibre RealTime provides direct calls to Calibre analysis engines running foundry-qualified Calibre

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Benefits

- Provides instantaneous feedback on signoff-level DRC violations during layout creation and editing
- Reduces verification iterations and overall design time
- Allows interactive editing of custom/AMS designs based on signoff-quality rule decks
- Enables design optimization during layout creation
- Integral part of design creation flow
- Increases designer productivity

Major Features

- Uses standard foundry-qualified Calibre rule decks
- Built-in error review toolbar enhances ease of use
- Automatically runs Calibre nmDRC whenever edits are made
- OpenAccess run-time model enables integration with most custom design environments
- In-memory checking ensures best performance
- User-defined custom filters tied to layout interface
- Complements existing built-in checkers
- Award-winning

rule decks. These Calibre engines perform fast, incremental checking in the vicinity of shapes being edited, providing nearly instantaneous feedback on design rule violations, as well as potential systematic variation susceptibility as measured by recommended rule compliance.

With its ability to perform all checks that can be run with Calibre DRC, including recommended rules, pattern matching, equation-based DRC, and double patterning, Calibre RealTime lets custom IC designers correct and adjust their designs during the layout process to produce a design that is DRC-clean, resistant to manufacturing variability issues, and optimized for the most desirable performance and operational characteristics.

Use Models

Cell-Level Design

At the cell level, designers can use Calibre RealTime's immediate feedback to optimize the design for performance during layout creation and editing, while continuing to use batch Calibre for library characterization and final signoff.

Analog/Custom Design

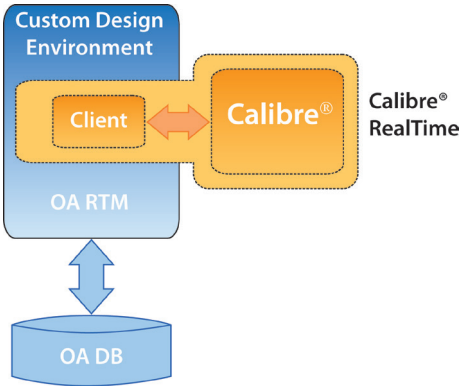
Analog and custom design engineers can take advantage of the nearly instantaneous feedback from Calibre RealTime to implement the highest quality designs possible. Because they can iterate through signoff-quality DRC while they design, they can be confident that the high performance design they create will also meet manufacturing standards.

DRC Repair for Full-Chip Verification

By combining Calibre RealTime with batch Calibre and Calibre RVE to identify and correct DRC violations during layout, designers can minimize the need for full-chip verification runs, shortening the production schedule when it is most critical—at tapeout.

Ease of Use

Calibre RealTime provides a tight integration between the Calibre physical verification platform and the custom IC design and layout system, based on the OpenAccess industry standard. Calibre DRC checking is transparently implemented, so users can begin enjoying the advantages of signoff quality DRC without the usual learning curve.



Calibre RealTime offers dynamic signoff-quality DRC to custom and analog/mixed-signal designers through the OpenAccess runtime model.

Calibre RealTime eliminates any gaps between the custom layout tool's built-in design rules and the foundry-qualified rule deck, so designers know they are getting accurate, up-to-date foundry information at the best possible time—while they are creating their design. At the same time, because it is integrated in addition to the built-in checker, users have the freedom to use either or both checking processes, as desired.

Calibre RealTime's built-in error review toolbar eliminates window clutter and enhances ease of use for custom designers. User-defined custom filters allow designers to limit which checks are run, based on design requirements and organizational processes, without having to modify the foundry-qualified rule deck.

Supported Integrations

- SpringSoft Laker™ version OA 2010.8
- Mentor Graphics IC Station® version v10

Superior Product Support

Mentor Graphics is a five-time winner of the Software Technical Assistance Recognition (STAR) Award in EDA. No other provider of complex software can match the support offered by Mentor Graphics.

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Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070-7777
Phone: 503-685-7000
Fax: 503-685-1204

Sales and Product Information
Phone: 800-547-3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

North American Support Center
Phone: 800-547-4303

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1001, 10F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-87252000
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140 -0001
Japan
Phone: 81-3-5488-3033
Fax: 81-3-5488-3004

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