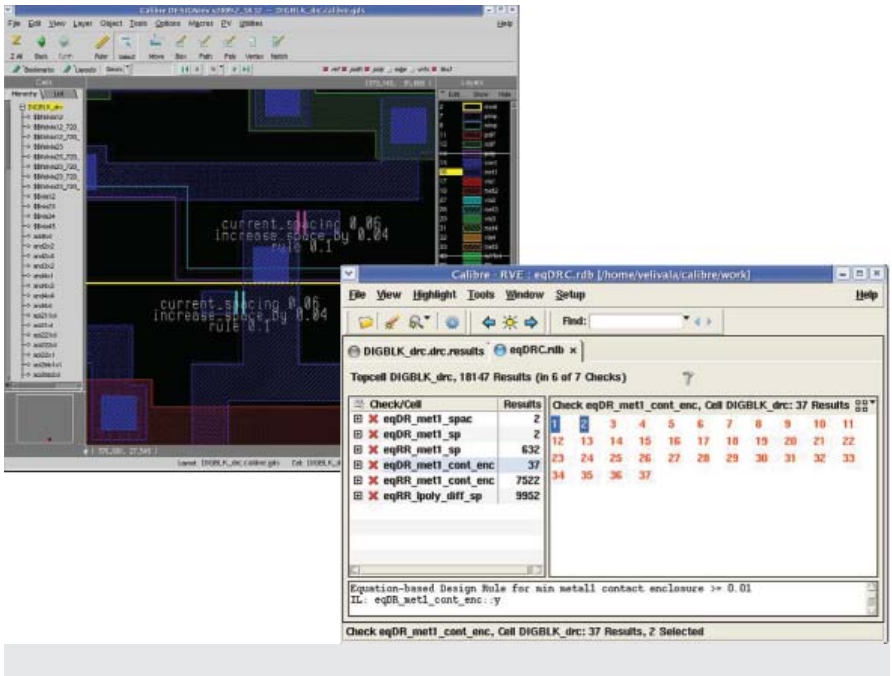
Physical Verification

Calibre RVE
Results Viewing Environment

D A T A S H E E T



Calibre RVE's robust viewing and debugging capabilities connect results from all Calibre tools back into your design or layout viewing environments for quick design closure.

Results Viewing Environment: Accelerating Time to Tape-Out

While the Calibre® platform's best-in-class engines provide physical and circuit verification results in record time, you still need to fix the identified layout issues before you can tape out. Calibre RVE™ provides fast, flexible, and easy-to-use graphical debugging capabilities that minimize your turnaround time and get you to "tapeout-clean" on schedule.

Calibre RVE is integrated into all the popular layout environments, including Mentor Graphics® IC Station®, Calibre DESIGNrev™, Synopsys® IC Compiler, Cadence® Encounter®, Cadence Virtuoso®, Springsoft Laker™, Seiko, Tanner, and Agilent ADS. Whatever design environment you use, Calibre RVE provides the debugging technology you need for fast, accurate error resolution.

Physical Verification

However complex the rule deck, Calibre RVE can handle it. Even with millions of error results, Calibre RVE provides fast navigation through the layout, allowing you to focus on analyzing and fixing the errors. The tabbed viewing format enables you to easily organize data by tiling the display windows side by side. And, because Calibre RVE is designed with a low-memory footprint, you can run it on the same machine you use for your design environment.

Key Product Benefits

- **Universal integration with layout environments:** Using Calibre RVE minimizes training and support overhead, and provides a single, consistent interface across all your design tools.
- **Fast debugging time for cell, block and full-chip designs:** Whether you have 10 or 10^6 errors, Calibre RVE provides fast response time with minimal memory overhead.
- **Single platform for all Calibre results:** Calibre RVE provides results debugging across the entire Calibre product line, giving you a single interface to learn and support for all your Calibre tools.
- **Reliability:** With thousands of users worldwide, Calibre RVE sets the standard for debug reliability and accuracy.
- **Schematics:** Visualizing the intended connectivity of the source schematic against the connectivity realized in the layout greatly speeds resolution of LVS errors.

Mentor Graphics®

Waived errors can be a source of needless work and lost time. Calibre RVE provides a flexible waiver flow to persistently mark, annotate, and review error results that will be waived by the foundry. Calibre RVE also provides integrated support for the Calibre Auto-Waiver flow and automatically removes waivers from the results, reducing your turnaround time even further.

Calibre RVE:

- Filters error results by cell, check, property, waived, and fixed status so you can quickly select only the results you want to review.
- Highlights DRC results in the context in which they occur, providing greater flexibility in error visualization, location and analysis.
- Marks and comments waived errors for subsequent DRC runs.
- Provides statistical summaries of error properties across checks and cells.
- Enables designers to merge generated polygons (such as metal fill) into the original layout database.

Circuit Verification

Calibre RVE has kept pace with the expanding requirements of circuit verification with a wide range of capabilities, including: layout vs. schematic (LVS), schematic vs. schematic (SVS), electrical rule checking (ERC), programmable electrical rule checking (PERC), soft checks, point-to-point resistance checking, and current density checking.

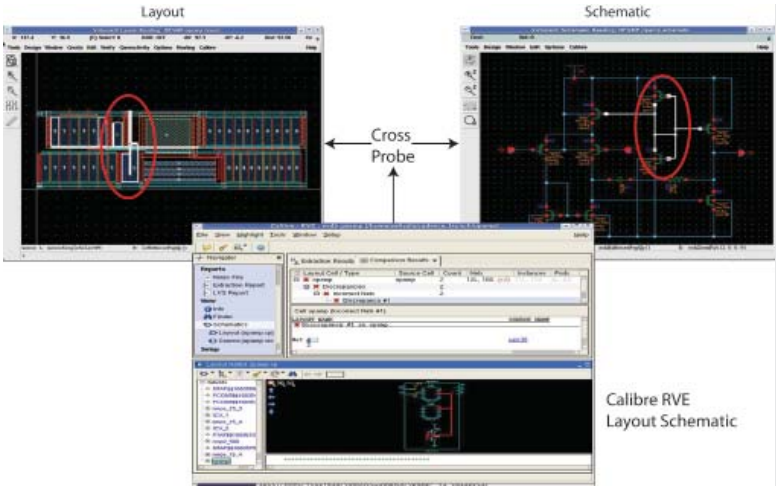
By providing both source and layout schematics, Calibre RVE can easily and quickly cross-highlight between the schematics, the design layout, and the Calibre LVS results report.

Calibre RVE circuit verification capabilities include:

- Fast and intuitive schematic visualization and hierarchical SPICE browser to navigate and highlight nets and devices. Highlights appear in layout and schematic windows, along with the Calibre RVE layout and source schematics.
- Fix suggestions that provide an English description of the error (e.g., “Layout net 5 and 10 are shorted”) to simplify and speed up the debugging process.
- Advanced Short Isolation function that can be run hierarchically and by layer to quickly isolate the root cause of a texted short. When the short isolation algorithm is unable to pinpoint the short, the Calibre RVE interface enables the user to interactively isolate the issue without re-running the batch tool.

Parasitic Extraction

Accurate timing and performance simulations for leading-edge circuit designs depend on accurate parasitic extraction. Using a tool such as Calibre xRC, with its industry-leading accuracy, to extract parasitics from the physical layout ensures high-quality results. Calibre RVE then enables you to quickly and easily navigate the extraction results, and perform both interactive and batch point-to-point calculations.



Calibre RVE offers dynamic cross-probing capabilities between layout, schematic, source netlist, layout netlist, and LVS result files.

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