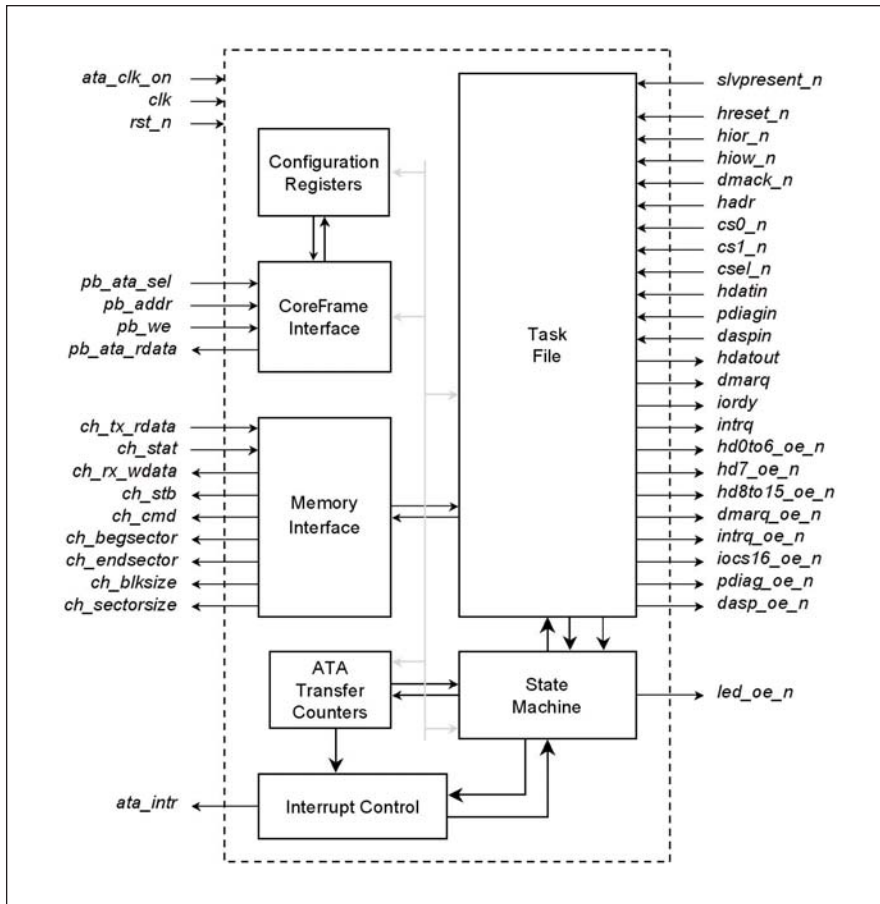


Parallel ATA IP

Device Controller

BK-3708

D A T A S H E E T



The Mentor Graphics parallel ATA device controller is designed to interface between a host system and a storage device.

Major product features:

- Supports ATA protocol
- Supports ATA-2 through ATA-6
- Programmable I/O modes: 0, 1, 2, 3, and 4
- Multi-word DMA modes: 0, 1, and 2
- Synchronous Ultra ATA-33, -66, -100, and -133 modes: 0, 1, 2, 3, 4, 5, and 6
- 28- or 48-bit LBA addressing
- Auto-read and auto-write
- Supports either CoreFrame or ARM AMBA AHB bus interface

Parallel ATA Device Controller

The Mentor Graphics® parallel ATA device controller is designed to interface between a host system and a storage controller in either solid state or rotating media.

The parallel ATA controller decodes an incoming host command and sets up the proper interrupts and status for the local microprocessor to handle various ATA commands. Many commands can be automated for full data transfer with minimal firmware support. Options also exist for full firmware handling of each phase of command handling. The parallel

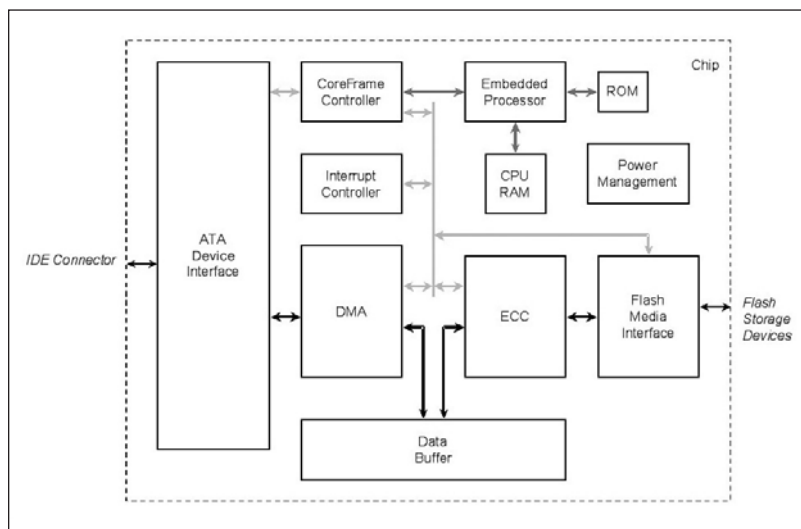
ATA device controller includes advanced features such as Ultra-ATA support and support for very large storage devices. This core has complete automation for ATA support. In addition, ATAPI support may be implemented through firmware.

The parallel ATA device controller is designed to interface to the local processor using either the CoreFrame® or the ARM AMBA AHB bus interface. It can be configured to support either an asynchronous or synchronous system interface.

Parallel ATA Device Controller Applications

The parallel ATA device core connects an IDE storage device to a host system with command interpretation handled by the target core in conjunction with an embedded processor.

The example below shows the ATA device core integrated into a solid-state storage device — a Flash card. The ATA device connects to the host system via a connector. Command processing is performed by interrupting the embedded processor. The processor parses the command and configures the various components to handle the command.



A solid state drive controller for the PC.

Data is transferred through the ATA device core into a data buffer via a DMA engine. ECC is calculated for the data and it is stored to the media under software direction. Data is read from the media, corrected via ECC if necessary, and transferred from the buffer to the host via the ATA core.

CoreFrame Bus Architecture

The CoreFrame bus architecture provides a high-performance interconnect scheme that allows silicon functional blocks to be combined quickly and easily. The architecture is independent of foundry, processor, and I/O. It supports 8-, 16-, and 32-bit peripherals.

Mentor Product and Technology Interoperability

Mentor's successful involvement in a variety of EDA technologies allows our IP customers to take full advantage of other Mentor technologies when the need arises. Integrating related Mentor technologies, such as embedded software,

0-In[®] checkers and monitors, and hardware emulation, offers IP customers a more seamless and cost-effective path to product success and enables customers to efficiently address the ever-changing dynamics of the industry.

World-Class Support from Mentor

Mentor Graphics is the only EDA company to receive the exclusive STAR (Software Technical Assistance Recognition) Life-Time Achievement Award — *five times*. This award-winning customer support division works closely with customers throughout the world and is dedicated to the entire design cycle.

IP Standards Compliance

Mentor Graphics actively supports key industry standards and protocols for successful IP integration. Mentor has significant involvement in the following standards bodies: IEEE-Ethernet 802.3; USB-IF; ASI SIG; SATA International Organization, and the VSIA Alliance.

Visit www.mentor.com/ip for additional IP product news and information.

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