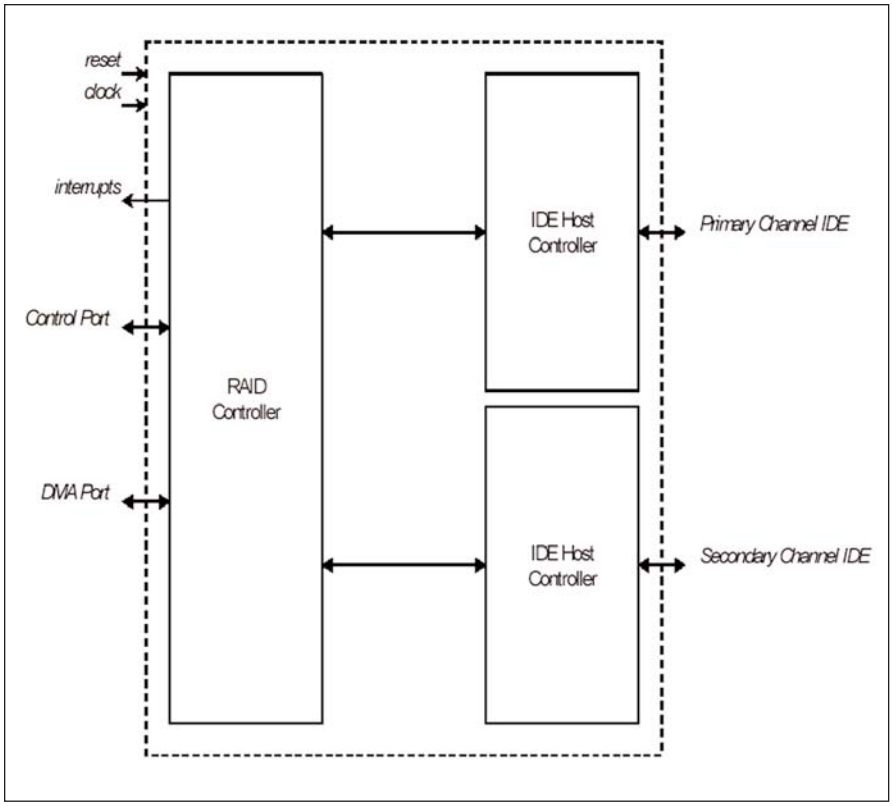
Parallel ATA IP

Host Controller with RAID and SpeedSelect

BK-3710SR

D A T A S H E E T



Block diagram of parallel ATA controller with built-in hardware RAID.

Parallel ATA Host Controller with RAID and SpeedSelect

The Mentor Graphics® parallel ATA host controller with RAID comprises two IDE controllers and a RAID controller. It provides an efficient and easy-to-use interface to up to 4 IDE and ATAPI devices. When RAID functionality is disabled, the controller acts as a two-channel IDE host controller. When RAID is enabled, the RAID controller takes control of the two IDE controller subsystems. The two IDE cores implement programmable I/O, multi-word direct memory access (DMA), and Ultra ATA-33, -66, -100, and -133 modes of operation, and each of the IDE cores supports up to two devices. The core interface to the system-on-chip provides PIO access and DMA capability to optimize data transfers to and from the IDE devices.

For ease of integration, the parallel ATA host controller includes a register set compatible with the Intel chip set, including a descriptor-based, scatter-gather DMA core. This core is compatible with ATA-4 with Ultra ATA-33, -66, -100, and -133 extensions. However, single-word DMA is not supported.

IDE features:

- Programmable I/O modes: 0, 1, 2, 3, and 4
- Multi-word DMA modes: 0, 1, and 2
- Synchronous Ultra ATA-33, -66, -100, and -133 modes: 0, 1, 2, 3, 4, 5, and 6
- Can be configured as primary and secondary IDE controller
- SpeedSelect technology allows core timings to be reprogrammed to support any ATA speed and timing mode at any clock frequency
- Descriptor-based, scatter-gather DMA controller
- Intel register set compatible
- Support for synchronous or asynchronous DMA interface for data transfers
- Supports up to two devices with independent master/slave timing controls
- Supports either CoreFrame or ARM AMBA AHB bus interface

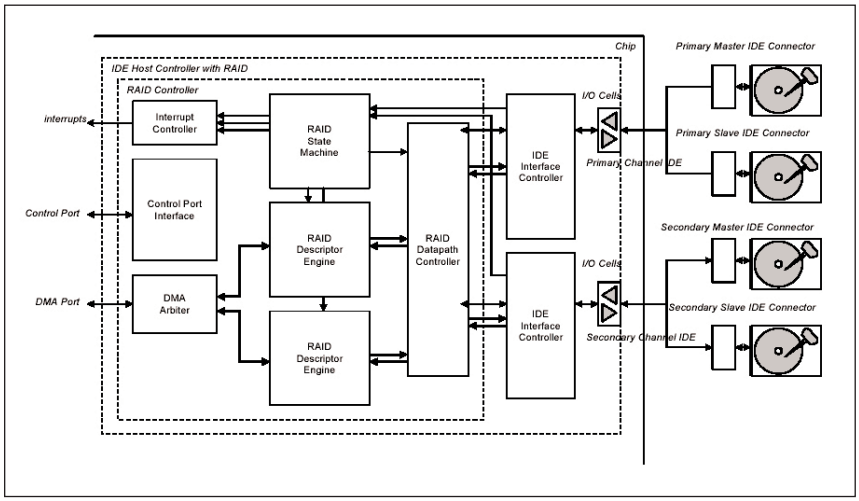
RAID features:

- Two-channel IDE controller with RAID disabled
- RAID 0 (stripping to primary/secondary)
- RAID 1 (mirroring to master/slave)
- RAID 0+1 (stripping to primary/secondary and mirroring to master/slave)
- RAID 3 (fixed parity drive)
- RAID 5 (rotating parity drive)
- Automatic redundancy generation on writes
- No redundancy checking on reads
- Support for hot spare
- Support for hot swap
- Support for 48-bit LBAs
- Software-driven array rebuild
- Software-driven data availability with incomplete array

The parallel host controller also contains a patent-pending SpeedSelect™ technology. This allows the core to be reconfigured to support any timing mode for PIO, multi-word DMA, and Ultra ATA transfers (-33, -66, -100, or -133) while running at any clock frequency. The core is designed to interface to the host processor and system memory using either the CoreFrame® or the ARM AMBA AHB bus interface. The core can be configured to support either an asynchronous or synchronous system interface.

Parallel ATA Host Controller with RAID Applications

The parallel ATA host controller is used to control IDE disk drives and the IDE host with RAID core is applicable to any system utilizing multiple IDE/ATA and ATAPI drives for data storage, including desktop computers, servers, set-top boxes, and test equipment. The parallel ATA host controller is suitable for use with all form factor IDE/ATA and ATAPI drives. The example below shows the IDE host with RAID core used in a desktop computer. The application supports four drives by instantiating two IDE host controller blocks; one controller is configured as a primary port controller; the second controller is configured as a secondary port controller.



Example of BK-3710SR in PC application.

The core includes a scatter-gather DMA channel compatible with the Intel scatter-gather DMA engine.

The parallel ATA host controller with RAID core interfaces to two pairs of IDE drives, allowing simultaneous access to two IDE drives and support for up to four IDE drives. One pair comprises the primary channel and the other pair comprises the secondary channel. In the configuration where each drive has its own connector, four presence detect pins are available.

CoreFrame Bus Architecture

The CoreFrame architecture provides a high-performance interconnect scheme that allows silicon functional blocks to be combined quickly and easily. The architecture is independent of foundry, processor, and I/O. It supports 8-, 16-, and 32-bit peripherals.

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Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1603, 16F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

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