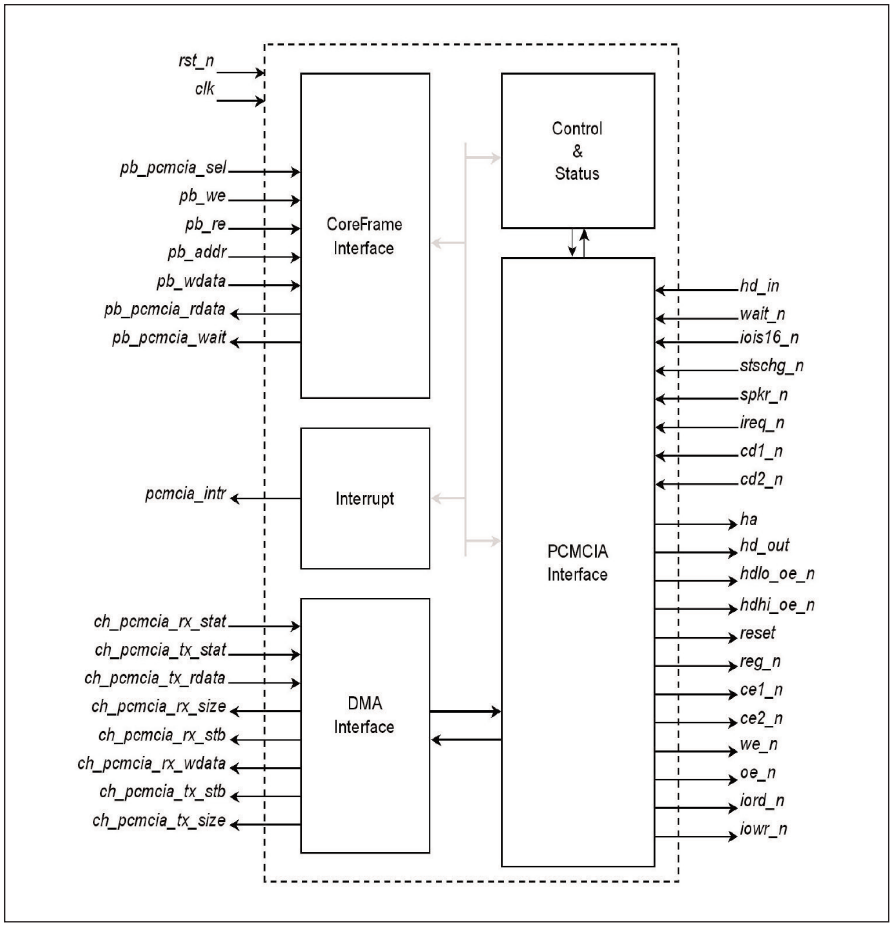
PCMCIA IP

Host Controller

BK-3712

D A T A S H E E T



The Mentor Graphics PCMCIA host controller is designed to interface to the processor through a CoreFrame bus interface.

Major product features:

- Supports memory and I/O modes
- Supports 8-bit and 16-bit accesses
- Up to 20 MB/s transfer rate in common memory mode
- Up to 17 MB/s transfer rate in PIO mode
- Conforms to PCMCIA card 2.1 standard
- Data transfer to/from memory via DMA or PIO interface
- 133 MHz maximum operating frequency in 0.18u
- Supports either CoreFrame or ARM AMBA AHB bus interface

PCMCIA Card Host Controller

The Mentor Graphics PCMCIA core provides an efficient and easy-to-use interface to devices that are PCMCIA card 2.1 compliant. The core generates read/write cycles for attribute memory, common memory, and I/O modes.

The core is designed to interface to the processor through a CoreFrame® bus interface. The CoreFrame bus interface is a non-pipelined interface incorporating address, data, read strobe, write strobe, and a wait signal. Interrupt status and masking registers are provided to enable polled or interrupt driven firmware to service the interrupts. Particular events on the PCMCIA card interface can be programmed to generate an interrupt to the processor. The core includes programmable timing control registers to support a wide range of operating frequencies. PC cards can be memory mapped to simplify firmware.

Expansion Capabilities

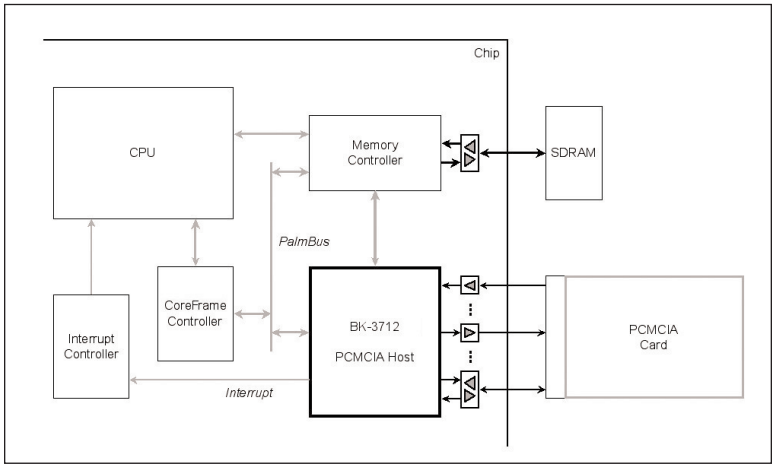
The PCMCIA host controller provides expansion capability through the use of standard removable PCMCIA card devices. The host controller allows direct PIO access to cards, and direct memory access (DMA) for large, high-speed data transfers with a minimum of CPU intervention.

The example below shows the PCMCIA host core used to interface to a PCMCIA card. This application is commonly used to add product features after the device has been manufactured (adding wired or wireless networking capability, for example) and to provide removable storage, such as Flash cards and compact Flash cards. Applications for add-on capability include home gateways and palm-sized PC devices. Applications for removable storage include digital imaging devices and palm-sized PCs.

The PCMCIA host communicates to the PCMCIA card through a standard 40-pin connector. Direct access to the external card is performed via the CoreFrame bus, as is control and configuration of the core. For large data transfers, the DMA port may be used to transfer data directly to system memory — the core interrupts the CPU when transfer is complete.

CoreFrame Architecture

The CoreFrame architecture provides a high-performance interconnect scheme that allows silicon functional blocks to be combined quickly and easily. The architecture is independent of foundry, processor, and I/O. It supports 8-, 16-, 32-, and 64-bit peripherals.



The PCMCIA host core integrated into an SoC environment.

About Mentor Graphics Silicon-Proven, Standards-Based Intellectual Property

Mentor Graphics offers a variety of industry-leading, standards-based IP cores that are rigorously tested and validated to provide design teams with the most reliable cores in the industry. Mentor's IP portfolio ranges from simple SoC building blocks, such as communications interfaces and microcontrollers, to an expansive offering of products for Ethernet, USB, Storage, and PCI Express.

Visit www.mentor.com/ip for more information on our complete IP portfolio of Storage, Ethernet, USB, and PCI Express products.

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