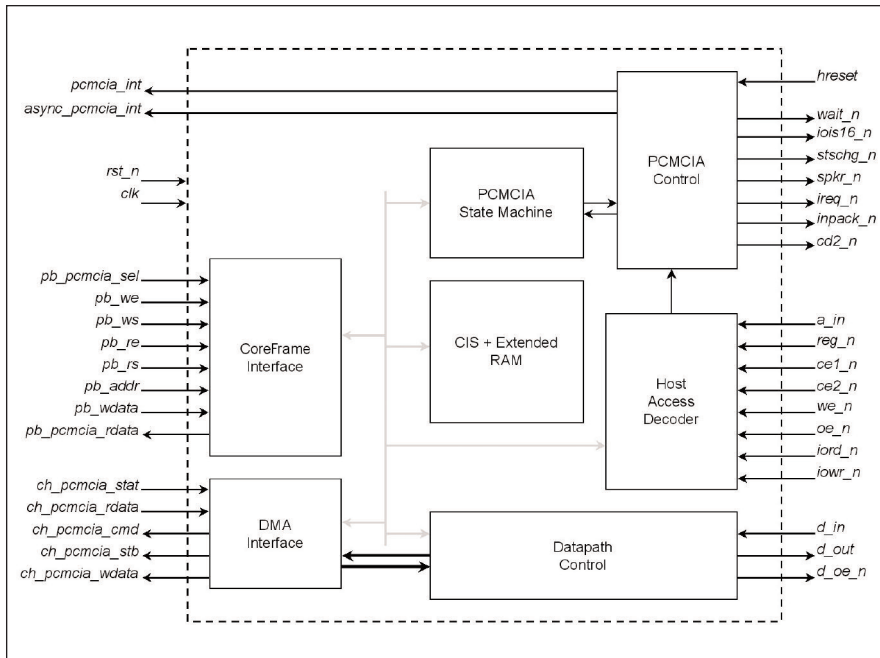


# PCMCIA IP

## Device Controller

BK-3713

D A T A S H E E T



The Mentor Graphics PCMCIA device controller is designed to interface to the processor through the CoreFrame or ARM AMBA AHB bus interface.

### Major product features:

- Supports memory and I/O modes
- Up to 20 MB/s transfer rate in common memory mode
- Up to 17 MB/s transfer rate in PIO mode
- Conforms to PCMCIA card 2.1 standard
- Data transfer to/from memory via DMA or PIO interfaces
- 256-byte CIS RAM
- 256-byte PIO RAM
- PCMCIA registers accessible in low-power state
- 133 MHz maximum operating frequency in 0.18u
- Supports either CoreFrame or ARM AMBA AHB bus interface

### PCMCIA Card Device Controller

The Mentor Graphics PCMCIA core provides PCMCIA card 2.1 compliance to SoC devices. The core is capable of responding to cycles for attribute memory, common memory, and I/O modes up to the maximum rate allowed by the PCMCIA standard.

The core is designed to interface to the processor through the CoreFrame® or AHB interface. Direct memory access (DMA) is provided through a FIFO-like interface to an external DMA channel. The CoreFrame bus is a non-pipelined interface incorporating address, data, read strobe, write strobe, and a wait signal. The DMA channel interface is a non-pipelined interface that includes FIFO status, data, and read and write strobes. Interrupt status and masking registers allow polled or interrupt-driven firmware to service interrupt events.

On-board CIS RAM holds all required card information, and is available to the host system in any power mode. The host can access the card via PIO for command sequences and via DMA for large data transfers. The card's memory map to the host is programmable, allowing for flexible operation in any application.

### Industry-Standard Interface

The PCMCIA device controller provides an industry-standard interface for adding removable expansion capabilities to many systems, including mobile and consumer products.

The example on the next page shows the PCMCIA device core used in a PCMCIA card. PCMCIA is commonly used to add product features after the device has been manufactured (adding wired or wireless networking capability, for example) and to provide removable storage, such as Flash storage.

Applications for add-on capability include modems and wired or wireless networking. Applications for removable storage include digital image processing and storage.

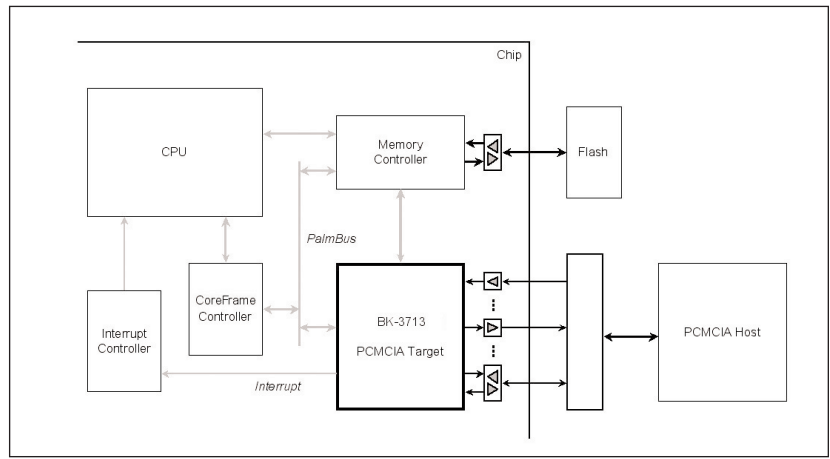
The PCMCIA device core communicates to the host system through a standard 68-pin connector, to a local processor via the CoreFrame bus, and to memory via a DMA port. The controller is operable in a low power state so it can be recognized and configured by the host and can interrupt the local processor to exit low-power mode when needed.

### CoreFrame Architecture

The CoreFrame architecture provides a high-performance interconnect scheme that allows silicon functional blocks to be combined quickly and easily. The architecture is independent of foundry, processor, and I/O. It supports 8-, 16-, 32-, and 64-bit peripherals.

### About Mentor Graphics Silicon-Proven, Standards-Based Intellectual Property

Mentor Graphics offers a variety of industry-leading, standards-based IP cores that are rigorously tested and validated to provide design teams with the most reliable cores in the industry. Mentor's IP portfolio ranges from simple SoC building blocks, such as communications interfaces and microcontrollers, to an expansive offering of products for Ethernet, USB, Storage, and PCI Express.



The PCMCIA host core integrated into an SoC environment.

Visit [www.mentor.com/ip](http://www.mentor.com/ip) for more information on our complete IP portfolio of Storage, Ethernet, USB, and PCI Express products.

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