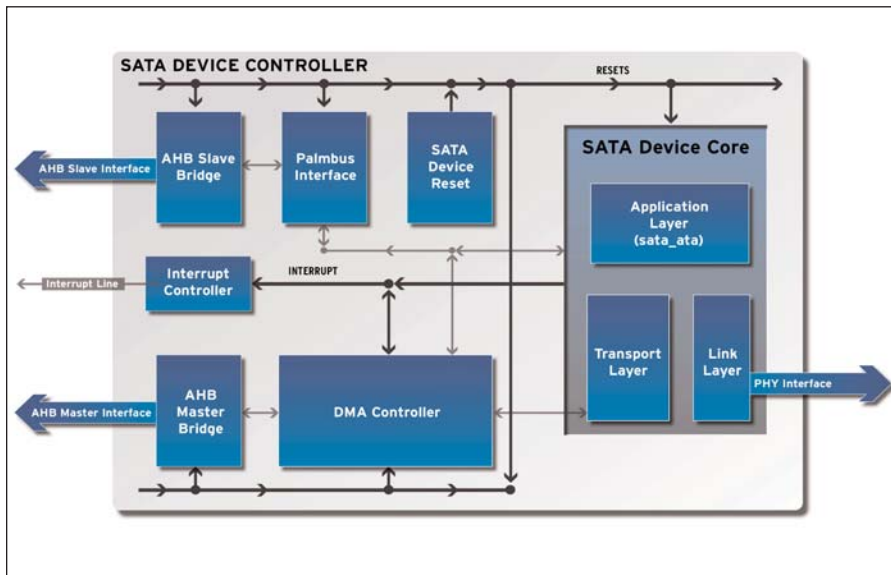


Serial ATA IP - Device Controller



The Mentor Graphics Serial ATA Device Controller with optional direct memory access controller (DMA).

SATA Device Controller Integrated with Optional DMA

The Mentor Graphics® Serial ATA (SATA) Device Controller is designed to interface between a host system and a storage device with either solid state or rotating media.

The SATA Device Controller decodes incoming host commands and sets up the proper interrupts and status for the local microprocessor to handle ATA and ATAPIO commands. The controller can be programmed to automatically transfer the data with minimal firmware support interfaces: a control interface and a direct memory access (DMA) interface. This SATA Device Controller supports either the CoreFrame or the AMBA AHB 2.0 bus interface.

Major product features:

- Compliant with the Serial ATA specification version 2.6
- Supports 1.5 Gb/s (150 MB/s) or 3 Gb/s (300 MB/s) speeds
- Software-compatible with parallel ATA
- Supports Native Command Queuing (NCQ)
- Support for Spread Spectrum Clocking (SSC)
- Auto-read and auto-write
- Integrated DMA controller
- Supports 20-bit SATA standard PHY interface
- Asynchronous Notification
- Supports either CoreFrame or AMBA AHB 2.0 bus interface

Deliverables:

- Verilog RTL source code
- Example synthesis scripts
- Verilog functional verification environment with task-based verification and PHY model
- Detailed specifications including user guide, product specification, verification guide, and programmers guide

Related products:

- **MSATA PHY S130A** - SATA PHY (up to 3Gbps) for SMIC 130nmG
- **MSATA PHY T130A** - SATA PHY (up to 3Gbps) for TSMC 130nm LVOD

Signal Interface Signals

System Interface Signals		
Signal	Type	Description
SYS_CLK	Input	System Clock
SATA_CLK	Input	SATA Clock (75Mhz or 150Mhz)
TESTMODE	Input	Scan Test mode
RST_N	Input	Power on Reset
SPD_CONF	Input	Interface Speed Configuration
ATA_INTR	Output	Interrupt Signal
AHB_ERROR	Output	AHB Interface Error Flag (debug)
HRST_N	Output	Hard Reset Interrupt
AHB Master Interface Signals		
HRDATA_M[31:0]	Input	AHB Master Read Data Bus
HREADY	Input	AHB Master Ready
HGRANT_M	Input	AHB Master Bus Grant
HRESP_M[1:0]	Input	AHB Master Transfer Response
HBUSREQ_M	Output	AHB Master Bus Request
HADDR_M[31:0]	Output	AHB Master Address Bus
HWDATA_M[31:0]	Output	AHB Master Write Data Bus
HWRITE_M	Output	AHB Master Write Signal
HSIZE_M[2:0]	Output	AHB Master Burst Size
HBURST_M[2:0]	Output	AHB Master Burst Type
HTRANS_M[1:0]	Output	AHB Master Transfer Type
HLOCK_M	Output	AHB Master Bus Request Lock
AHB Slave Interface Signals		
HADDR_S[31:0]	Input	AHB Slave Address Bus
HWDATA_S[31:0]	Input	AHB Slave Write Data Bus
HTRANS_S[1:0]	Input	AHB Slave Transfer Type
HSEL_S	Input	AHB Slave Select Line
HWRITE_S	Input	AHB Slave Write Signal
HSIZE_S[2:0]	Input	AHB Slave Burst Size
HRDATA_S[31:0]	Output	AHB Slave Read Data Bus
HREADY_OUT	Output	AHB Slave Output Ready Line
HRESP_S[1:0]	Output	AHB Slave Transfer Response
PHY Interface Signals		
RXCLOCK	Input	Receive Data Clock
PL_DATA [19:0]	Input	Receive Data
PHYRDY	Input	PHYRDY Signal Detected
COMWAKE	Input	COMWAKE Detected
COMINIT	Input	COMINIT Detected
SPDMODE	Input	Speed Setting
LP_DATA [19:0]	Output	Transmit Data
PHYRESET_N	Output	PHY Reset Signal
SPDSEL	Output	Speed Setting Output
FARAFELB	Output	Serial Loopback Enable
PARTIAL	Output	Partial Power Mode Enable
SLUMBER	Output	Slumber Power Mode Enable

data between a device system and a SATA Physical Layer such as the MSATA PHY product from Mentor Graphics.

The Link Controller interacts directly with the SATA PHY to coordinate serial transfers. It generates and checks CRC, scrambles/descrambles data, performs encoding/decoding, and manages primitive transmission and receipt.

The Transport Layer is used to store the headers of incoming and outgoing packets. Data, Status, and Vendor-specific Packet Headers sent to and from the device are stored in the FIS buffers, which are part of the Transport Layer.

The Application Layer decodes incoming host commands and sets up the proper interrupts and status for the local microprocessor to handle the ATA commands. The hardware will automatically perform the initial handshake with the host during read and write commands. When auto-transfer mode is enabled, read and write transfers can be fully handled by hardware with minimal firmware interaction.

Reference Technology Gate Count:
• 25,000 gates

Functional Description

The SATA Device Controller is designed to interface to a device CPU and DMA interface on one end, and the SATA Physical Layer on the other end. The Application Layer Controller, the

Transport Layer Controller, and the Link Layer Controller are the three core submodules that control the overall operation.

The three controllers coordinate their actions and utilize resources to transfer

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